ADC161S626 16-Bit, 50 to 250 kSPS, Differential Input, MicroPower ADC

Check for Samples: ADC161S626

FEATURES

- **16-bit resolution with no missing codes**
- **Guaranteed performance from 50 to 250 kSPS**
- **±0.003% signal span accuracy**
- **Separate Digital Input/Output Supply**
- **True differential input**
- **External voltage reference range of +0.5V to V_A**
- **Zero-Power Track Mode with 0 µsec wake-up delay**
- **Wide input common-mode voltage range of 0V to V_A**
- **SPI™/QSPI™/MICROWIRE™ compatible Serial Interface**
- **Operating temperature range of −40°C to +85°C**
- **Small MSOP-10 package**

APPLICATIONS

- **Direct Sensor Interface**
- **I/O Modules**
- **Data Acquisition**
- **Portable Systems**
- **Motor Control**
- **Medical Instruments**
- **Instrumentation and Control Systems**

DESCRIPTION

The ADC161S626 is a 16-bit successive-approximation register (SAR) Analog-to-Digital converter (ADC) with a maximum sampling rate of 250 kSPS. The ADC161S626 has a minimum signal span accuracy of ± 0.003% over the temperate range of −40°C to +85°C. The converter features a differential analog input with an excellent common-mode signal rejection ratio of 85 dB, making the ADC161S626 suitable for noisy environments.

The ADC161S626 operates with a single analog supply (V_A) and a separate digital input/output (V_{IO}) supply. V_A can range from +4.5V to +5.5V and V_{IO} can range from +2.7V to +5.5V. This allows a system designer to maximize performance and minimize power consumption by operating the analog portion of the ADC at a V_A of +5V while interfacing with a +3.3V controller. The serial data output is binary 2's complement and is SPI™ compatible.

The performance of the ADC161S626 is guaranteed over temperature at clock rates of 1 MHz to 5 MHz and reference voltages of +2.5V to +5.5V. The ADC161S626 is available in a small 10-lead MSOP package. The high accuracy, differential input, low power consumption, and small size make the ADC161S626 ideal for direct connection to bridge sensors and transducers in battery operated systems or remote data acquisition applications.

Table 1. Key Specifications

		VALUE	UNIT
Conversion Rate		50 kSPS to 250 kSPS	
DNL		+ 0.8 / − 0.5	LSB
INL		± 0.8	LSB
Offset Error Temp Drift		2.5 µV/°C	
Gain Error Temp Drift		0.3 ppm/°C	
SNR		93.2	dBc
THD		− 104	dBc
Power Consumption			
	10 kSPS, 5V	0.24	mW
	200 kSPS, 5V	5.3	mW

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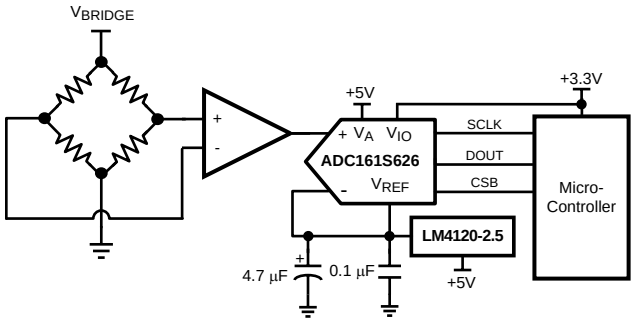
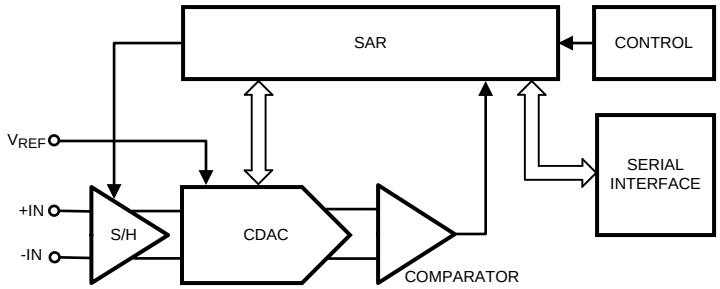
Table 1. Key Specifications (continued)

	250 kSPS, 5V	5.8	mW
	Power-Down, 5V	10 µW	

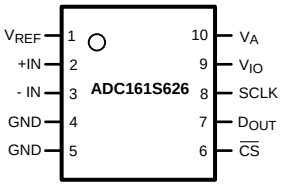
Typical Application



Block Diagram



Connection Diagram



Pin Functions

Pin Descriptions

Pin No.	Symbol	Description
1	V_{REF}	Voltage Reference +0.5V < V_{REF} < V_A
2	+IN	Non-Inverting Input
3	−IN	Inverting Input
4	GND	Ground
5	GND	Ground
6	$\overline{CS}$	Chip Select Bar
7	D_{OUT}	Serial Data Output
8	SCLK	Serial Clock
9	V_{IO}	Digital Input/Output Power +2.7V < V_{REF} < +5.5V

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Pin Descriptions (continued)

Pin No.	Symbol	Description
10	V_A	Analog Power +4.5V < V_{REF} < +5.5V

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1) (2)

Analog Supply Voltage V_A	−0.3V to 6.5V
Digital I/O Supply Voltage V_{IO}	−0.3V to 6.5V
Voltage on Any Analog Input Pin to GND	−0.3V to (V_A + 0.3V)
Voltage on Any Digital Input Pin to GND	−0.3V to (V_{IO} + 0.3V)
Input Current at Any Pin (3)	±10 mA
Package Input Current (3)	±50 mA
Power Consumption at T_A = 25°C	See (4)
ESD Susceptibility (5) Human Body Model Machine Model Charge Device Model	 2500V 250V 1250V
Junction Temperature	+150°C
Storage Temperature	−65°C to +150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions. Operation of the device beyond the maximum Operating Ratings is not recommended.
(2) All voltages are measured with respect to GND = 0V, unless otherwise specified.
(3) When the input voltage at any pin exceeds the power supplies (that is, V_{IN} < GND or V_{IN} > V_A), the current at that pin should be limited to 10 mA. The 50 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 10 mA to five.
(4) The absolute maximum junction temperature ($T_J$max) for this device is 150°C. The maximum allowable power dissipation is dictated by $T_J$max, the junction-to-ambient thermal resistance (θ_{JA}), and the ambient temperature (T_A), and can be calculated using the formula $P_D MAX = (T_J max - T_A)/\theta_{JA}$. The values for maximum power dissipation listed above will be reached only when the ADC161S626 is operated in a severe fault condition (e.g. when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Such conditions should always be avoided.
(5) Human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor. Machine model is a 220 pF capacitor discharged through 0 Ω. Charge device model simulates a pin slowly acquiring charge (such as from a device sliding down the feeder in an automated assembler) then rapidly being discharged.

Operating Ratings (1) (2)

Operating Temperature Range	−40°C ≤ T_A ≤ +85°C
Supply Voltage, V_A	+4.5V to +5.5V
Supply Voltage, V_{IO}	+2.7V to +5.5V
Reference Voltage, V_{REF}	+0.5V to V_A
Analog Input Pins Voltage Range	0V to V_A
Differential Analog Input Voltage	−V_{REF} to +V_{REF}
Input Common-Mode Voltage, V_{CM}	See Figure 10
Digital Input Pins Voltage Range	0V to V_{IO}
Clock Frequency	1 MHz to 5 MHz

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions. Operation of the device beyond the maximum Operating Ratings is not recommended.
(2) All voltages are measured with respect to GND = 0V, unless otherwise specified.

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Package Thermal Resistance

Package	θ_{JA}
10-lead MSOP	240°C / W

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ADC161S626 Converter Electrical Characteristics (1)

The following specifications apply for V_A = 4.5V to 5.5V, V_{IO} = 2.7V to 5.5V, and V_{REF} = 2.5V to 5.5V for f_{SCLK} = 1 MHz to 4 MHz or V_{REF} = 4.5V to 5.5V for f_{SCLK} = 1 MHz to 5 MHz; f_{IN} = 20 kHz, and C_L = 25 pF, unless otherwise noted. Maximum and minimum values apply for $T_A = T_{MIN}$ to T_{MAX}; the typical values are tested at T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC CONVERTER CHARACTERISTICS						
	Resolution with No Missing Codes				16	Bits
DNL	Differential Non-Linearity		−1	-0.5/+0.8	+2	LSB
INL	Integral Non-Linearity		−2	±0.8	+2	LSB
OE	Offset Error	V_{REF} = 2.5V	−1	−0.1	+1	mV
		V_{REF} = 5V		−0.4		mV
OE_{DRIFT}	Offset Error Temperature Drift	V_{REF} = 2.5V		3.7		µV/°C
		V_{REF} = 5V		2.5		µV/°C
FSE	Positive Full-Scale Error			−0.003	±0.03	%FS
	Negative Full-Scale Error			−0.002	±0.03	%FS
GE	Positive Gain Error			−0.002	±0.02	%FS
	Negative Gain Error			−0.0001	±0.02	%FS
GE_{DRIFT}	Gain Error Temperature Drift			0.3		ppm/°C
DYNAMIC CONVERTER CHARACTERISTICS						
SINAD	Signal-to-Noise Plus Distortion Ratio	V_{REF} = 2.5V	85	88		dBc
		V_{REF} = 4.5V to 5.5V	89	93.0		dBc
SNR	Signal-to-Noise Ratio	V_{REF} = 2.5V	85	88		dBc
		V_{REF} = 4.5V to 5.5V	89	93.2		dBc
THD	Total Harmonic Distortion	V_{REF} = 2.5V		−104		dBc
		V_{REF} = 4.5V to 5.5V		−106		dBc
SFDR	Spurious-Free Dynamic Range	V_{REF} = 2.5V		108		dBc
		V_{REF} = 4.5V to 5.5V		111		dBc
ENOB	Effective Number of Bits	V_{REF} = 2.5V	13.8	14.3		bits
		V_{REF} = 4.5V to 5.5V	14.5	15.2		bits
FPBW	−3 dB Full Power Bandwidth	Output at 70.7%FS with FS Differential Input		26		MHz
ANALOG INPUT CHARACTERISTICS						
V_{IN}	Differential Input Range		$-V_{REF}$		$+V_{REF}$	V
I_{INA}	Analog Input Current	$\overline{CS}$ high			±1	µA
		V_{REF} = 5V, V_{IN} = 0V, f_S = 50 kSPS		3.2		nA
		V_{REF} = 5V, V_{IN} = 0V, f_S = 200 kSPS		10.3		nA
C_{INA}	Input Capacitance (+IN or −IN)	In Acquisition Mode		20		pF
		In Conversion Mode		4		pF
CMRR	Common Mode Rejection Ratio	See the Specification Definitions for the test condition		85		dB
DIGITAL INPUT CHARACTERISTICS						
V_{IH}	Input High Voltage	f_{IN} = 0 Hz	0.7 x V_{IO}	1.9		V
V_{IL}	Input Low Voltage	f_{IN} = 0 Hz		1.7	0.3 x V_{IO}	V
I_{IND}	Digital Input Current				±1	µA
C_{IND}	Input Capacitance				4	pF
DIGITAL OUTPUT CHARACTERISTICS						
V_{OH}	Output High Voltage	I_{SOURCE} = 200 µA	V_{IO} − 0.2	V_{IO} − 0.03		V
		I_{SOURCE} = 1 mA		V_{IO} − 0.09		V

(1) Typical values are at T_J = 25°C and represent most likely parametric norms. Test limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

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ADC161S626 Converter Electrical Characteristics (1) (continued)

The following specifications apply for V_A = 4.5V to 5.5V, V_{IO} = 2.7V to 5.5V, and V_{REF} = 2.5V to 5.5V for f_{SCLK} = 1 MHz to 4 MHz or V_{REF} = 4.5V to 5.5V for f_{SCLK} = 1 MHz to 5 MHz; f_{IN} = 20 kHz, and C_L = 25 pF, unless otherwise noted. Maximum and minimum values apply for $T_A = T_{MIN}$ to T_{MAX}; the typical values are tested at T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OL}	Output Low Voltage	I_{SOURCE} = 200 µA		0.01	0.4	V
		I_{SOURCE} = 1 mA		0.07		V
I_{OZH}, I_{OZL}	TRI-STATE Leakage Current	Force 0V or V_A			±1	µA
C_{OUT}	TRI-STATE Output Capacitance	Force 0V or V_A		4		pF
	Output Coding			Binary 2'S Complement		
POWER SUPPLY CHARACTERISTICS						
V_A	Analog Supply Voltage Range		4.5	5	5.5	V
V_{IO}	Digital Input/Output Supply Voltage Range	(2)	2.7	3	5.5	V
V_{REF}	Reference Voltage Range		0.5	5	V_A	V
I_{VA} (Conv)	Analog Supply Current, Conversion Mode	V_A = 5V, f_{SCLK} = 4 MHz, f_S = 200 kSPS		1060		µA
		V_A = 5V, f_{SCLK} = 5 MHz, f_S = 250 kSPS		1160	1340	µA
I_{VIO} (Conv)	Digital I/O Supply Current, Conversion Mode	V_{IO} = 3V, f_{SCLK} = 4 MHz, f_S = 200 kSPS		80		µA
		V_{IO} = 3V, f_{SCLK} = 5 MHz, f_S = 250 kSPS		100		µA
I_{VREF} (Conv)	Reference Current, Conversion Mode	V_A = 5V, f_{SCLK} = 4 MHz, f_S = 200 kSPS		80		µA
		V_A = 5V, f_{SCLK} = 5 MHz, f_S = 250 kSPS		100	170	µA
I_{VA} (PD)	Analog Supply Current, Power Down Mode ($\overline{CS}$ high)	f_{SCLK} = 5 MHz, V_A = 5V		7		µA
		f_{SCLK} = 0 Hz, V_A = 5V (3)		2	3	µA
I_{VIO} (PD)	Digital I/O Supply Current, Power Down Mode ($\overline{CS}$ high)	f_{SCLK} = 5 MHz, V_{IO} = 3V		1		µA
		f_{SCLK} = 0 Hz, V_{IO} = 3V (3)		0.3	0.5	µA
I_{VREF} (PD)	Reference Current, Power Down Mode ($\overline{CS}$ high)	f_{SCLK} = 5 MHz, V_{REF} = 5V		0.5		µA
		f_{SCLK} = 0 Hz, V_{REF} = 5V (3)		0.5	0.7	µA
PWR (Conv)	Power Consumption, Conversion Mode	V_A = 5V, f_{SCLK} = 4 MHz, f_S = 200 kSPS, and f_{IN} = 20 kHz,		5.3		mW
		V_A = 5V, f_{SCLK} = 5 MHz, f_S = 250 kSPS, and f_{IN} = 20		5.8	6.7	mW
PWR (PD)	Power Consumption, Power Down Mode ($\overline{CS}$ high)	f_{SCLK} = 5 MHz, V_A = 5.0V (3)		35		µW
		f_{SCLK} = 0 Hz, V_A = 5.0V (3)		10	15	µW
PSRR	Power Supply Rejection Ratio	See the Specification Definitions for the test condition		−78		dB
AC ELECTRICAL CHARACTERISTICS						
f_{SCLK}	Maximum Clock Frequency		1		5	MHz
f_S	Maximum Sample Rate	(4)	50		250	kSPS
t_{ACQ}	Acquisition/Track Time		600			ns
t_{CONV}	Conversion/Hold Time				17	SCLK cycles
t_{AD}	Aperture Delay	See the Specification Definitions		6		ns

(2) The value of V_{IO} is independent of the value of V_A. For example, V_{IO} could be operating at 5.5V while V_A is operating at 4.5V or V_{IO} could be operating at 2.7V while V_A is operating at 5.5V.
(3) This parameter is guaranteed by design and/or characterization and is not tested in production.
(4) While the maximum sample rate is f_{SCLK} / 20, the actual sample rate may be lower than this by having the $\overline{CS}$ rate slower than f_{SCLK} / 20.

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ADC161S626 Timing Specifications (1)

The following specifications apply for V_A = 4.5V to 5.5V, V_{IO} = 2.7V to 5.5V, V_{REF} = 2.5V to 5.5V, f_{SCLK} = 1Mz to 5MHz, and C_L = 25 pF, unless otherwise noted. Maximum and minimum values apply for $T_A = T_{MIN}$ to T_{MAX}; the typical values are tested at T_A = 25°C.

Symbol	Parameter	Min	Typ	Max	Units
t_{CSS}	$\overline{CS}$ Setup Time prior to an SCLK rising edge	8	3		ns
t_{CSH}	$\overline{CS}$ Hold Time after an SCLK rising edge	8	3		
t_{DH}	D_{OUT} Hold Time after an SCLK falling edge	6	11		ns
t_{DA}	D_{OUT} Access Time after an SCLK falling edge		18	41	ns
t_{DIS}	D_{OUT} Disable Time after the rising edge of $\overline{CS}$ (2)		20	30	ns
t_{CS}	Minimum $\overline{CS}$ Pulse Width	20			ns
t_{EN}	D_{OUT} Enable Time after the 2nd falling edge of SCLK		20	70	ns
t_{CH}	SCLK High Time	20			ns
t_{CL}	SCLK Low Time	20			ns
t_r	D_{OUT} Rise Time		7		ns
t_f	D_{OUT} Fall Time		7		ns

(1) Typical values are at T_J = 25°C and represent most likely parametric norms. Test limits are guaranteed to National's AOQL (Average Outgoing Quality Level).
(2) t_{DIS} is the time for D_{OUT} to change 10% while being loaded by the Timing Test Circuit.

Timing Diagrams

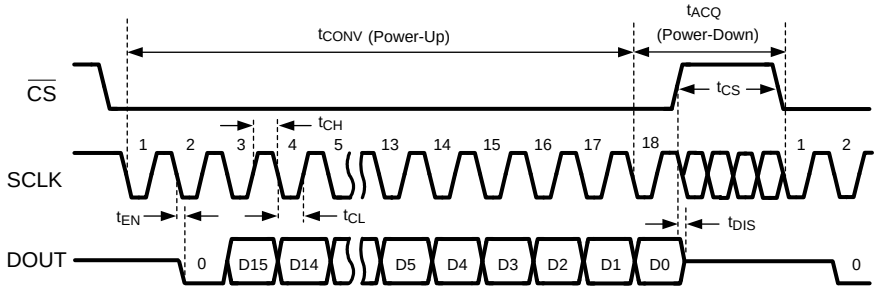

Figure 1. ADC161S626 Single Conversion Timing Diagram

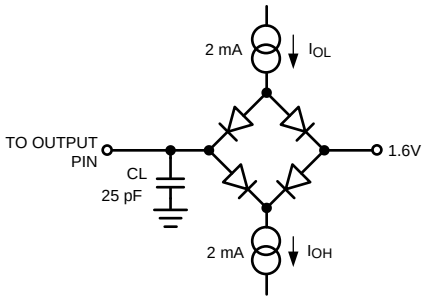

Figure 2. Timing Test Circuit

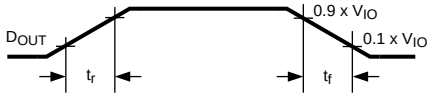

Figure 3. D_{OUT} Rise and Fall Times

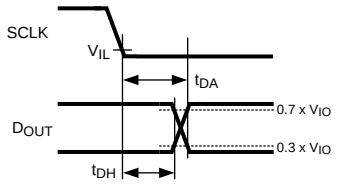

Figure 4. D_{OUT} Hold and Access Times

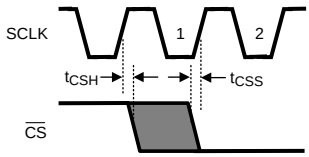

Figure 5. Valid $\overline{CS}$ Assertion Times

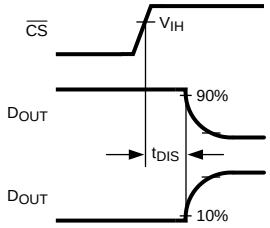

Figure 6. Voltage Waveform for t_{DIS}

Specification Definitions

APERTURE DELAY is the time between the first falling edge of SCLK and the time when the input signal is sampled for conversion.

COMMON MODE REJECTION RATIO (CMRR) is a measure of how well in-phase signals common to both input pins are rejected.

To calculate CMRR, the change in output offset is measured while the common mode input voltage is changed from 2V to 3V.

CMRR = 20 LOG (Δ Common Input / Δ Output Offset) (1)

CONVERSION TIME is the time required, after the input voltage is acquired, for the ADC to convert the input voltage to a digital word.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB.

DUTY CYCLE is the ratio of the time that a repetitive digital waveform is high to the total time of one period. The specification here refers to the SCLK.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion or SINAD. ENOB is defined as (SINAD − 1.76) / 6.02 and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

FULL POWER BANDWIDTH is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

GAIN ERROR is the deviation from the ideal slope of the transfer function. It is the difference between Positive Full-Scale Error and Negative Full-Scale Error and can be calculated as:

Gain Error = Positive Full-Scale Error − Negative Full-Scale Error (2)

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INTEGRAL NON-LINEARITY (INL) is a measure of the deviation of each individual code from a line drawn from ½ LSB below the first code transition through ½ LSB above the last code transition. The deviation of any given code from this straight line is measured from the center of that code value.

MISSING CODES are those output codes that will never appear at the ADC outputs. The ADC161S626 is guaranteed not to have any missing codes.

NEGATIVE FULL-SCALE ERROR is the difference between the differential input voltage at which the output code transitions from code 0x8001h to 0x8000h and $-V_{REF}$ + 1 LSB.

NEGATIVE GAIN ERROR is the difference between the negative full-scale error and the offset error.

OFFSET ERROR is the difference between the differential input voltage at which the output code transitions from code 0x0000h to 0x0001h and 1 LSB.

POSITIVE FULL-SCALE ERROR is the difference between the differential input voltage at which the output code transitions from code 0xFFFEh to 0xFFFFh and V_{REF} - 1 LSB.

POSITIVE GAIN ERROR is the difference between the positive full-scale error and the offset error.

POWER SUPPLY REJECTION RATIO (PSRR) is a measure of how well a change in the analog supply voltage is rejected. PSRR is calculated from the ratio of the change in offset error for a given change in supply voltage, expressed in dB. For the ADC161S626, V_A is changed from 4.5V to 5.5V.

$$PSRR = 20 \text{ LOG } (\Delta \text{Output Offset} / \Delta V_A) \quad (3)$$

SIGNAL TO NOISE RATIO (SNR) is the ratio, expressed in dB, of the rms value of the input signal to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or d.c.

SIGNAL TO NOISE PLUS DISTORTION (S/N+D or SINAD) Is the ratio, expressed in dB, of the rms value of the input signal to the rms value of all of the other spectral components below one-half the sampling frequency, including harmonics but excluding d.c.

SPURIOUS FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the desired signal amplitude to the amplitude of the peak spurious spectral component below one-half the sampling frequency, where a spurious spectral component is any signal present in the output spectrum that is not present at the input and may or may not be a harmonic.

TOTAL HARMONIC DISTORTION (THD) is the ratio of the rms total of the first five harmonic components at the output to the rms level of the input signal frequency as seen at the output, expressed in dB. THD is calculated as

$$THD = 20 \times \log_{10} \sqrt{\frac{A_{f2}^2 + \Lambda + A_{f6}^2}{A_{f1}^2}} \quad (4)$$

where A_{f1} is the RMS power of the input frequency at the output and A_{f2} through A_{f6} are the RMS power in the first 5 harmonic frequencies.

THROUGHPUT TIME is the minimum time required between the start of two successive conversion.

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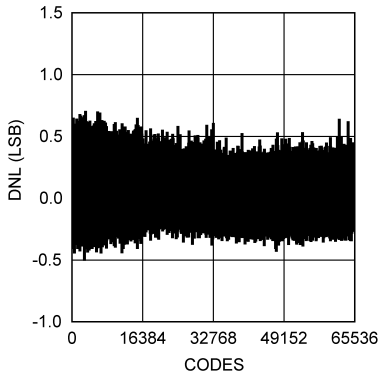
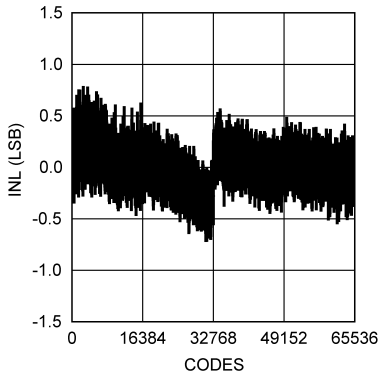
Typical Performance Characteristics

$V_A = V_{IO} = V_{REF} = +5V$, $f_{SCLK} = 5$ MHz, $f_{SAMPLE} = 250$ kSPS, $T_A = +25°C$, and $f_{IN} = 20$ kHz unless otherwise stated.

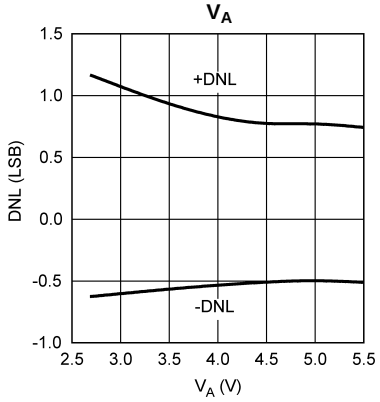
DNL - 250 kSPS



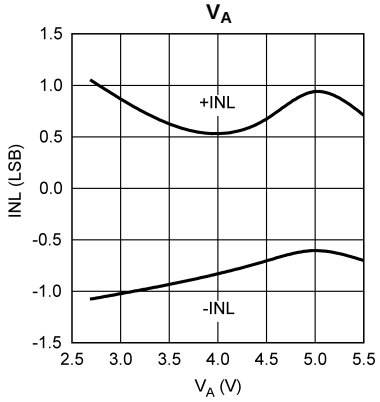
INL - 250 kSPS



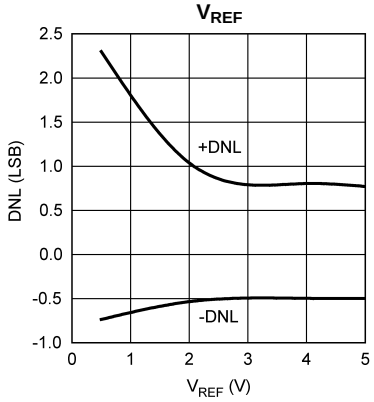
DNL vs. V_A



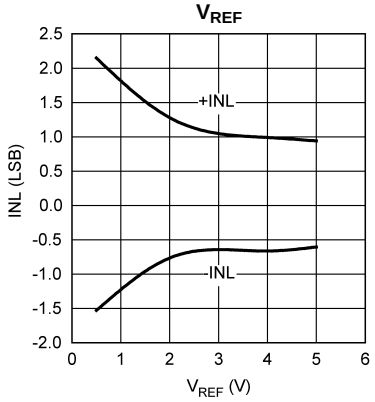
INL vs. V_A



DNL vs. V_{REF}



INL vs. V_{REF}



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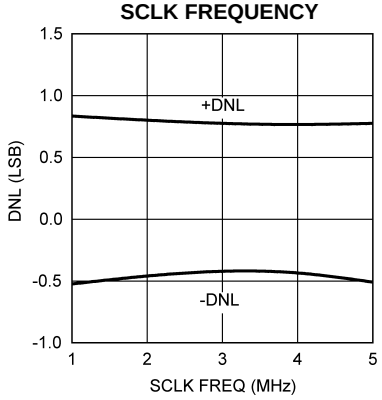
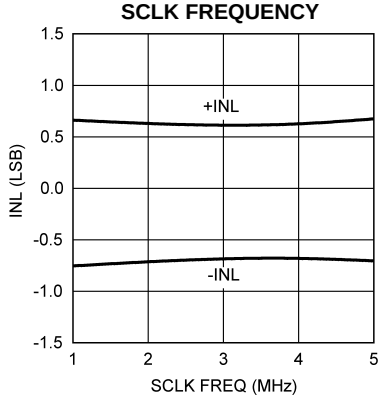
Typical Performance Characteristics

$V_A = V_{IO} = V_{REF} = +5V$, $f_{SCLK} = 5$ MHz, $f_{SAMPLE} = 250$ kSPS, $T_A = +25°C$, and $f_{IN} = 20$ kHz unless otherwise stated.

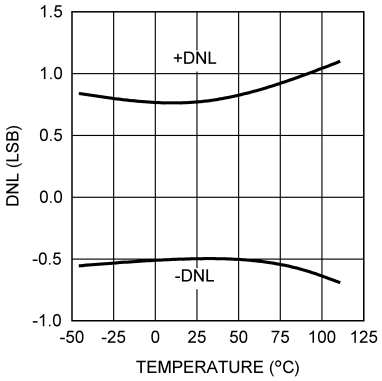
DNL vs. SCLK FREQUENCY



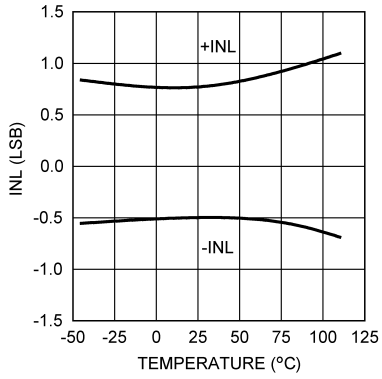
INL vs. SCLK FREQUENCY



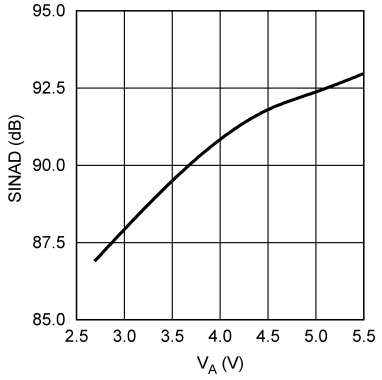
DNL vs. TEMPERATURE



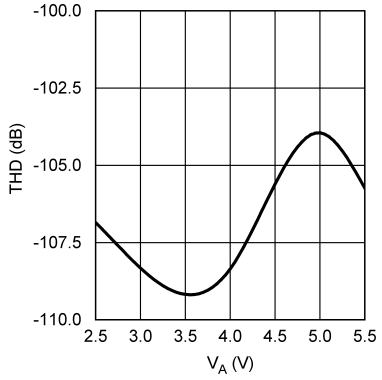
INL vs. TEMPERATURE



SINAD vs. V_A



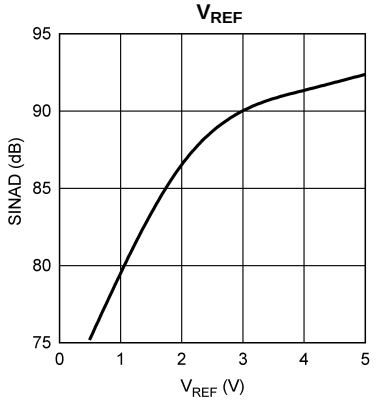
THD vs. V_A



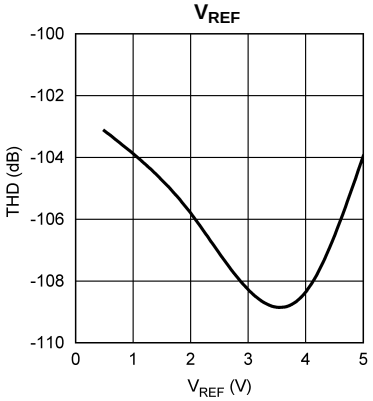
Typical Performance Characteristics

$V_A = V_{IO} = V_{REF} = +5V$, $f_{SCLK} = 5$ MHz, $f_{SAMPLE} = 250$ kSPS, $T_A = +25°C$, and $f_{IN} = 20$ kHz unless otherwise stated.

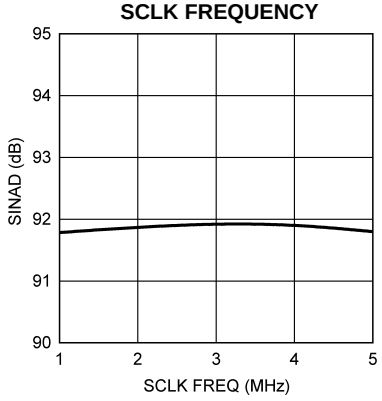
SINAD vs. V_{REF}



THD vs. V_{REF}



SINAD vs. SCLK FREQUENCY



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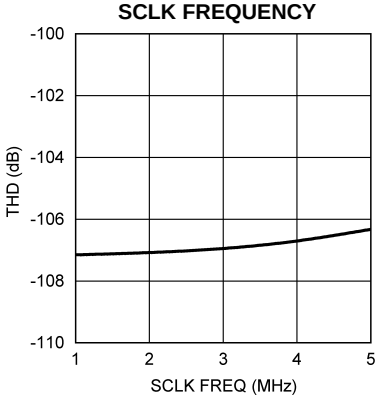
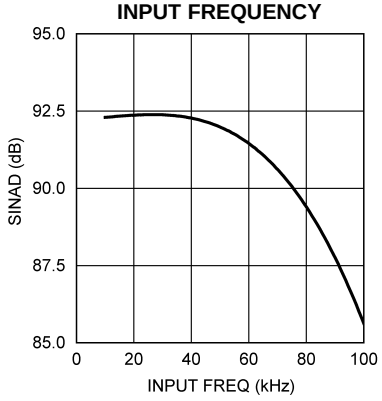
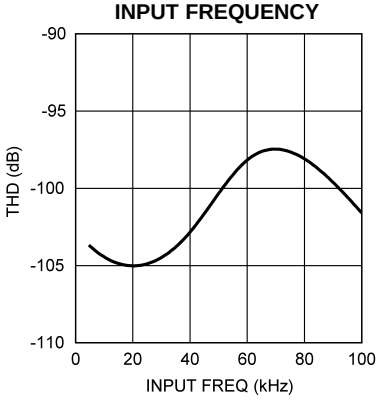


SINAD vs. INPUT FREQUENCY



THD vs. INPUT FREQUENCY



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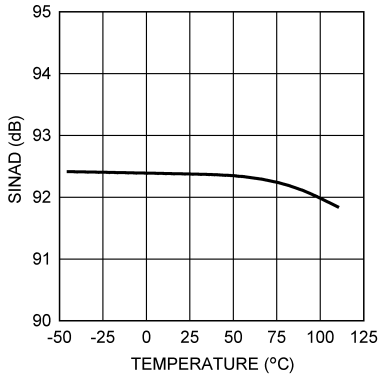
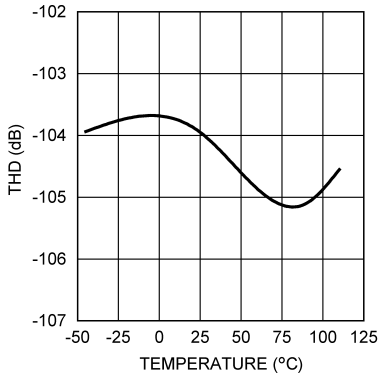
Typical Performance Characteristics

$V_A = V_{IO} = V_{REF} = +5V$, $f_{SCLK} = 5$ MHz, $f_{SAMPLE} = 250$ kSPS, $T_A = +25°C$, and $f_{IN} = 20$ kHz unless otherwise stated.

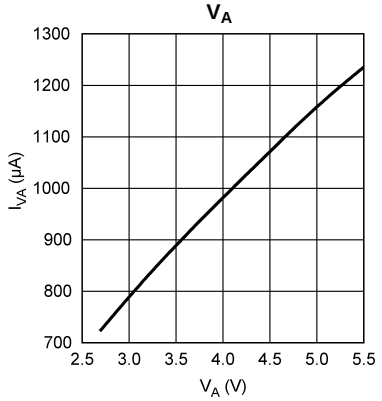
SINAD vs. TEMPERATURE



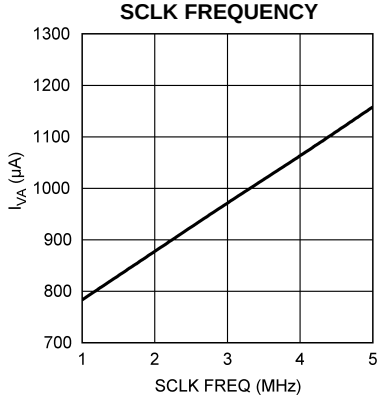
THD vs. TEMPERATURE



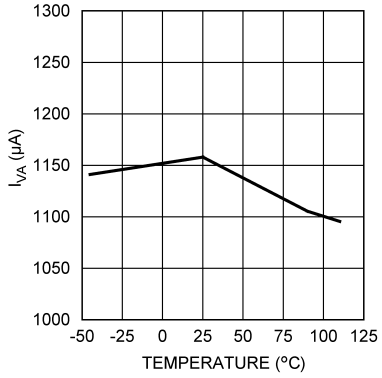
V_A CURRENT vs. V_A



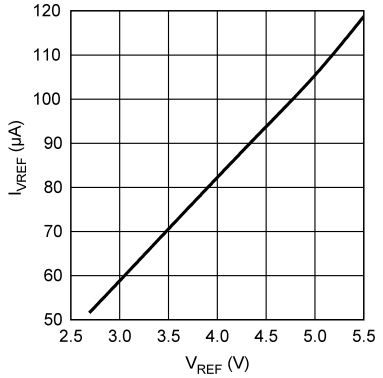
V_A CURRENT vs. SCLK FREQUENCY



V_A CURRENT vs. TEMPERATURE



V_{REF} CURRENT vs. V_{REF}



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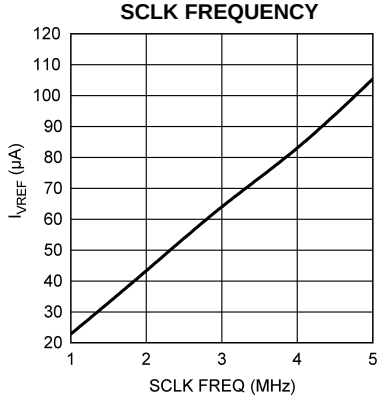
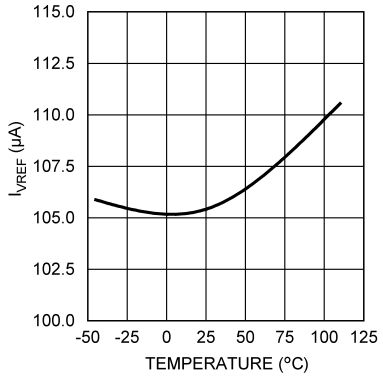
Typical Performance Characteristics

$V_A = V_{IO} = V_{REF} = +5V$, $f_{SCLK} = 5$ MHz, $f_{SAMPLE} = 250$ kSPS, $T_A = +25°C$, and $f_{IN} = 20$ kHz unless otherwise stated.

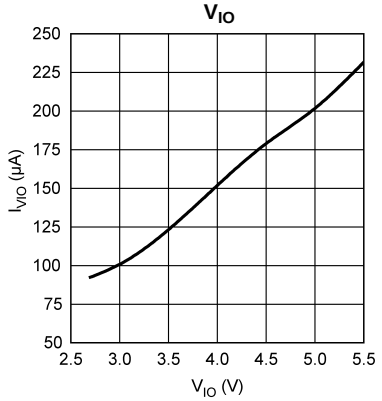
V_{REF} CURRENT vs. SCLK FREQUENCY



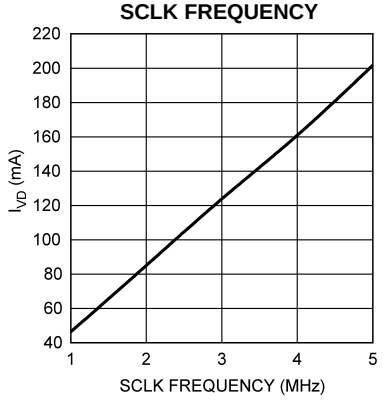
V_{REF} CURRENT vs. TEMPERATURE



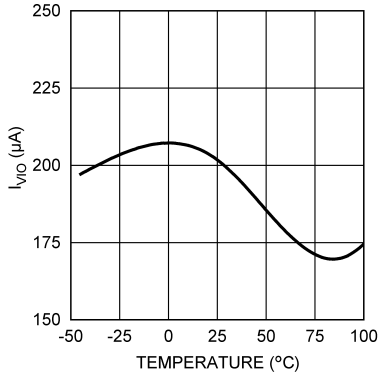
V_{IO} CURRENT vs. V_{IO}



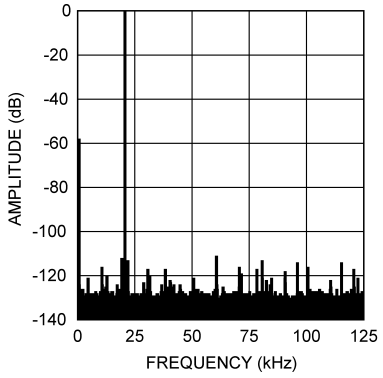
V_{IO} CURRENT vs. SCLK FREQUENCY



V_{IO} CURRENT vs. TEMPERATURE



SPECTRAL RESPONSE - 250 kSPS



Functional Description

The ADC161S626 is a 16-bit, 50 kSPS to 250 kSPS sampling Analog-to-Digital (A/D) converter. The converter uses a successive approximation register (SAR) architecture based upon capacitive redistribution containing an inherent sample-and-hold function. The differential nature of the analog inputs is maintained from the internal sample-and-hold circuits throughout the A/D converter to provide excellent common-mode signal rejection.

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The ADC161S626 operates from independent analog and digital supplies. The analog supply (V_A) can range from 4.5V to 5.5V and the digital input/output supply (V_{IO}) can range from 2.7V to 5.5V. The ADC161S626 utilizes an external reference (V_{REF}), which can be any voltage between 0.5V and V_A. The value of V_{REF} determines the range of the analog input, while the reference input current (I_{REF}) depends upon the conversion rate.

The analog input is presented to two input pins: +IN and –IN. Upon initiation of a conversion, the differential input at these pins is sampled on the internal capacitor array. The inputs are disconnected from the internal circuitry while a conversion is in progress. The ADC161S626 features a zero-power track mode (ZPTM) where the ADC is consuming the minimum amount of power (Power-Down Mode) while the internal sampling capacitor array is tracking the applied analog input voltage. The converter enters ZPTM at the end of each conversion window and experiences no delay when the ADC enters into Conversion Mode. This feature allows the user an easy means for optimizing system performance based on the settling capability of the analog source while minimizing power consumption. ZPTM is exercised by bringing chip select bar ($\overline{CS}$) high or when $\overline{CS}$ is held low after the conversion is complete (after the 18th falling edge of the serial clock).

The ADC161S626 communicates with other devices via a Serial Peripheral Interface (SPI™), a synchronous serial interface that operates using three pins: chip select bar ($\overline{CS}$), serial clock (SCLK), and serial data out (D_{OUT}). The external SCLK controls data transfer and serves as the conversion clock. The duty cycle of SCLK is essentially unimportant, provided the minimum clock high and low times are met. The minimum SCLK frequency is set by internal capacitor leakage. Each conversion requires a minimum of 18 SCLK cycles to complete. If less than 16 bits of conversion data are required, $\overline{CS}$ can be brought high at any point during the conversion. This procedure of terminating a conversion prior to completion is commonly referred to as short cycling.

The digital conversion result is clocked out by the SCLK input and is provided serially, most significant bit (MSB) first, at the D_{OUT} pin. The digital data that is provided at the D_{OUT} pin is that of the conversion currently in progress and thus there is no pipe line delay or latency.

REFERENCE INPUT (V_{REF})

The externally supplied reference voltage (V_{REF}) sets the analog input range. The ADC161S626 will operate with V_{REF} in the range of 0.5V to V_A.

Operation with V_{REF} below 2.5V is possible with slightly diminished performance. As V_{REF} is reduced, the range of acceptable analog input voltages is reduced. Assuming a proper common-mode input voltage (V_{CM}), the differential peak-to-peak input range is limited to (2 x V_{REF}).

Reducing V_{REF} also reduces the size of the least significant bit (LSB). For example, the size of one LSB is equal to [(2 x V_{REF}) / 2^n], which is 152.6 µV where n is 16 bits and V_{REF} is 5V. When the LSB size goes below the noise floor of the ADC161S626, the noise will span an increasing number of codes and overall performance will suffer. Dynamic signals will have their SNR degrade; while, D.C. measurements will have their code uncertainty increase. Since the noise is Gaussian in nature, the effects of this noise can be reduced by averaging the results of a number of consecutive conversions.

V_{REF} and analog inputs (+IN and -IN) are connected to the capacitor array through a switch matrix when the input is sampled. Hence, I_{REF}, I_{+IN}, and I_{-IN} are a series of transient spikes that occur at a frequency dependent on the operating sample rate of the ADC161S626.

I_{REF} changes only slightly with temperature. See the curves, “Reference Current vs. SCLK Frequency” and “Reference Current vs. Temperature” in the Typical Performance Curves section for additional details.

ANALOG SIGNAL INPUTS

The ADC161S626 has a differential input where the effective input voltage that is digitized is (+IN) − (−IN).

Differential Input Operation

The transfer curve of the ADC161S626 for a fully differential input signal is shown in Figure 7. A positive full scale output code (0111 1111 1111 1111b or 7FFFh or 32,767d) will be obtained when (+IN) − (−IN) is greater than or equal to (V_{REF} − 1 LSB). A negative full scale code (1000 0000 0000 0000b or 8000h or -32,768d) will be obtained when [(+IN) − (−IN)] is less than or equal to (−V_{REF} + 1 LSB). This ignores gain, offset and linearity errors, which will affect the exact differential input voltage that will determine any given output code.

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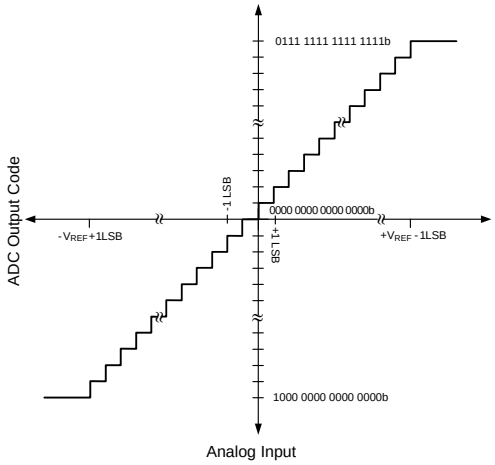

Figure 7. ADC Transfer Curve

Both inputs should be biased at a common mode voltage (V_{CM}), which will be thoroughly discussed in Figure 8 shows the ADC161S626 being driven by a full-scale differential source.

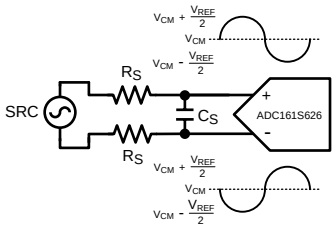

Figure 8. Differential Input

Single-Ended Input Operation

For single-ended operation, the non-inverting input (+IN) of the ADC161S626 can be driven with a signal that has a peak-to-peak range that is equal to or less than (2 x V_{REF}). The inverting input (−IN) should be biased at a stable V_{CM} that is halfway between these maximum and minimum values. In order to utilize the entire dynamic range of the ADC161S626, V_{REF} is limited to (V_A / 2). This allows +IN a maximum swing range of ground to V_A. Figure 9 shows the ADC161S626 being driven by a full-scale single-ended source.

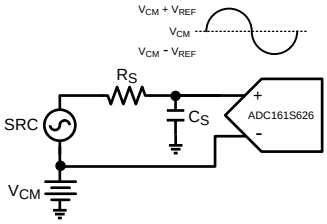

Figure 9. Single-Ended Input

Since the design of the ADC161S626 is optimized for a differential input, the performance degrades slightly when driven with a single-ended input. Linearity characteristics such as INL and DNL typically degrade by 0.1 LSB and dynamic characteristics such as SINAD typically degrade by 2 dB. Note that single-ended operation should only be used if the performance degradation (compared with differential operation) is acceptable.

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Input Common Mode Voltage

The allowable input common mode voltage (V_{CM}) range depends upon V_A and V_{REF} used for the ADC161S626. The ranges of V_{CM} are depicted in Figure 10 and Figure 11. Note that these figures only apply to a V_A of 5V. Equations for calculating the minimum and maximum V_{CM} for differential and single-ended operations are shown in Table 2.

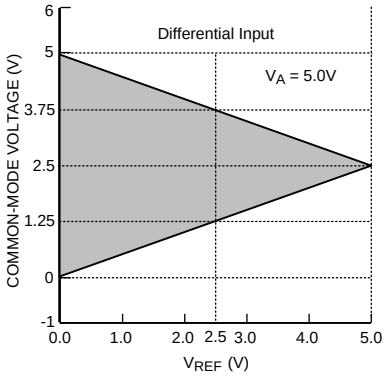

Figure 10. V_{CM} range for Differential Input operation

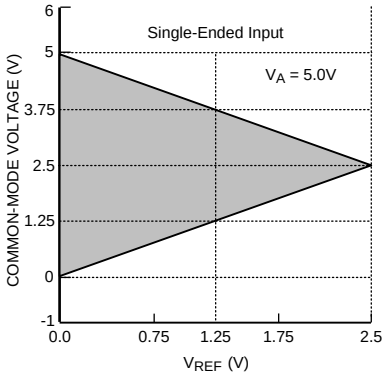

Figure 11. V_{CM} range for single-ended operation

Table 2. Allowable V_{CM} Range

Input Signal	Minimum V_{CM}	Maximum V_{CM}
Differential	V_{REF} / 2	V_A − V_{REF} / 2
Single-Ended	V_{REF}	V_A − V_{REF}

CMRR

By using this differential input, small signals common to both inputs are rejected. As shown in Figure 12, noise is immune at low frequencies where the common-mode rejection ratio (CMRR) is 90 dB. As the frequency increases to 1 MHz, the CMRR rolls off to 40 dB . In general, operation with a fully differential input signal or voltage will provide better performance than with a single-ended input. However, if desired, the ADC161S626 can be presented with a single-ended input.

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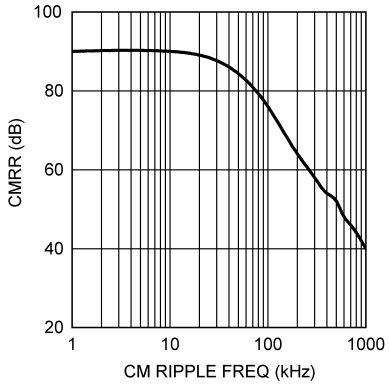

Figure 12. Analog Input CMRR vs. Frequency

Noise

The noise floor of the ADC161S626 is very low as shown in Figure 13 and Figure 14. These figures were created by driving the ADC input with a low-noise voltage source set near 0V. For Figure 13, the input was adjusted in order to obtain the code 0x0000h. For Figure 14, the input was increased by 1/2 LSB in order to obtain the transition point between code 0x0000h and 0x0001h. In both instances, 2^{16} (65,534) samples were collected and plotted in a histogram format.

Ideally the noise histogram at code center would show a single output code while the noise histogram at code transition would show two output codes. Any codes outside of the ideal output are a result of the internal noise of the ADC161S626 and the input source. Since the ADC161S626 has very low internal noise, only two codes outside of the center code are exhibited in the histogram of Figure 13. Similar results are shown in Figure 14.

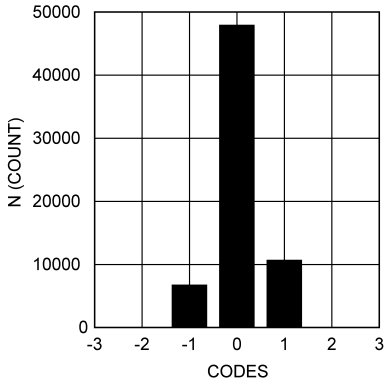

Figure 13. Noise Histogram at Code Center

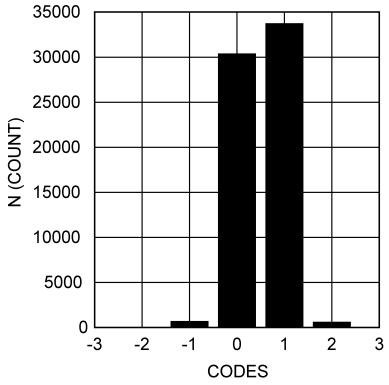

Figure 14. Noise Histogram at Code Transition

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Input Settling

When the ADC161S626 enters acquisition (t_{ACQ}) mode at the end of the conversion window, the internal sampling capacitor (C_{SAMPLE}) is connected to the ADC input via an internal switch and a series resistor (R_{SAMPLE}), as shown in Figure 15. Typical values for C_{SAMPLE} and R_{SAMPLE} are 20 pF and 200 ohms respectively. If there is not a large external capacitor (C_{EXT}) at the analog input of the ADC, a voltage spike will be observed at the input pins. This is a result of C_{SAMPLE} and C_{EXT} being at different voltage potentials. The magnitude and direction of the voltage spike depend on the difference between the voltage of C_{SAMPLE} and C_{EXT}. If the voltage at C_{SAMPLE} is greater than the voltage at C_{EXT}, a positive voltage spike will occur. If the opposite is true, a negative voltage spike will occur. It is not critical for the performance of the ADC161S626 to filter out the voltage spike. Rather, ensure that the transient of the spike settles out within t_{ACQ}; for recommended solutions, see Application Information.

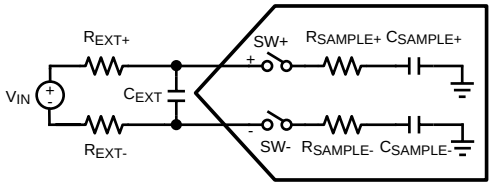

Figure 15. ADC Input Capacitors

SERIAL DIGITAL INTERFACE

The ADC161S626 communicates via a synchronous 3-wire serial interface as shown in Figure 1 or re-shown in Figure 16 for convenience. $\overline{CS}$, chip select bar, initiates conversions and frames the serial data transfers. SCLK (serial clock) controls both the conversion process and the timing of the serial data. D_{OUT} is the serial data output pin, where a conversion result is sent as a serial data stream, MSB first.

A serial frame is initiated on the falling edge of $\overline{CS}$ and ends on the rising edge of $\overline{CS}$. The ADC161S626's D_{OUT} pin is in a high impedance state when $\overline{CS}$ is high and for the first clock period after $\overline{CS}$ is asserted; D_{OUT} is active for the remainder of time when $\overline{CS}$ is asserted.

The ADC161S626 samples the differential input upon the assertion of $\overline{CS}$. Assertion is defined as bringing the $\overline{CS}$ pin to a logic low state. For the first 17 periods of the SCLK following the assertion of $\overline{CS}$, the ADC161S626 is converting the analog input voltage. On the 18th falling edge of SCLK, the ADC161S626 enters acquisition (t_{ACQ}) mode. For the next three periods of SCLK, the ADC161S626 is operating in acquisition mode where the ADC input is tracking the analog input signal applied across +IN and -IN. During acquisition mode, the ADC161S626 is consuming a minimal amount of power.

The ADC161S626 can enter conversion mode (t_{CONV}) under three different conditions. The first condition involves $\overline{CS}$ going low (asserted) with SCLK high. In this case, the ADC161S626 enters conversion mode on the first falling edge of SCLK after $\overline{CS}$ is asserted. In the second condition, $\overline{CS}$ goes low with SCLK low. Under this condition, the ADC161S626 automatically enters conversion mode and the falling edge of $\overline{CS}$ is seen as the first falling edge of SCLK. In the third condition, $\overline{CS}$ and SCLK go low simultaneously and the ADC161S626 enters conversion mode. While there is no timing restriction with respect to the falling edges of $\overline{CS}$ and SCLK, there are minimum setup and hold time requirements for the falling edge of $\overline{CS}$ with respect to the rising edge of SCLK. See Figure 5 in the Timing Diagram section for more information.

$\overline{CS}$ Input

The $\overline{CS}$ (chip select bar) input is active low and is CMOS compatible. The ADC161S626 enters conversion mode when $\overline{CS}$ is asserted and the SCLK pin is in a logic low state. When $\overline{CS}$ is high, the ADC161S626 is always in acquisition mode and thus consuming the minimum amount of power. Since $\overline{CS}$ must be asserted to begin a conversion, the sample rate of the ADC161S626 is equal to the assertion rate of $\overline{CS}$.

Proper operation requires that the fall of $\overline{CS}$ not occur simultaneously with a rising edge of SCLK. If the fall of $\overline{CS}$ occurs during the rising edge of SCLK, the data might be clocked out one bit early. Whether or not the data is clocked out early depends upon how close the $\overline{CS}$ transition is to the SCLK transition, the device temperature, and the characteristics of the individual device. To ensure that the MSB is always clocked out at a given time (the 3rd falling edge of SCLK), it is essential that the fall of $\overline{CS}$ always meet the timing requirement specified in the Timing Specification table.

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SCLK Input

The SCLK (serial clock) is used as the conversion clock to shift out the conversion result. SCLK is CMOS compatible. Internal settling time requirements limit the maximum clock frequency while internal capacitor leakage limits the minimum clock frequency. The ADC161S626 offers guaranteed performance with the clock rates indicated in the electrical table.

The ADC161S626 enters acquisition mode on the 18th falling edge of SCLK during a conversion frame. Assuming that the LSB is clocked into a controller on the 18th rising edge of SCLK, there is a minimum acquisition time period that must be met before a new conversion frame can begin. Other than the 18th rising edge of SCLK that was used to latch the LSB into a controller, there is no requirement for the SCLK to transition during acquisition mode. Therefore, it is acceptable to idle SCLK after the LSB has been latched into the controller.

Data Output

The data output format of the ADC161S626 is two's complement as shown in Figure 7. This figure indicates the ideal output code for a given input voltage and does not include the effects of offset, gain error, linearity errors, or noise. Each data output bit is output on the falling edges of SCLK. D_{OUT} is in a high impedance state for the 1st falling edge of SCLK while the 2nd SCLK falling edge clocks out a leading zero. The 3rd to 18th SCLK falling edges clock out the conversion result, MSB first.

While most receiving systems will capture the digital output bits on the rising edges of SCLK, the falling edges of SCLK may be used to capture the conversion result if the minimum hold time for D_{OUT} is acceptable. See Figure 4 for D_{OUT} hold (t_{DH}) and access (t_{DA}) times.

D_{OUT} is enabled on the second falling edge of SCLK after the assertion of $\overline{CS}$ and is disabled on the rising edge of $\overline{CS}$. If $\overline{CS}$ is raised prior to the 18th falling edge of SCLK, the current conversion is aborted and D_{OUT} will go into its high impedance state. A new conversion will begin when $\overline{CS}$ is driven LOW.

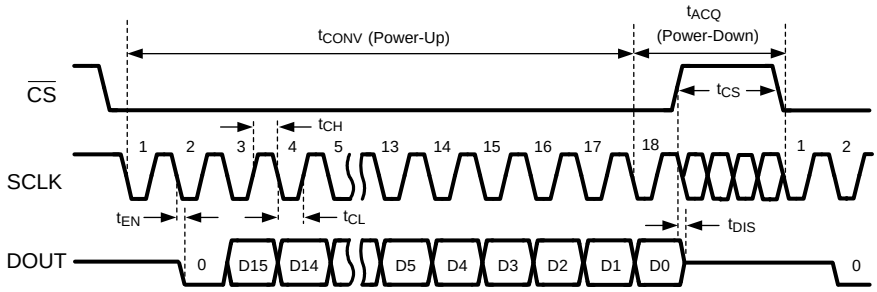

Figure 16. ADC161S626 Single Conversion Timing Diagram

Applications Information

OPERATING CONDITIONS

We recommend that the following conditions be observed for operation of the ADC161S626:

$-40°C \le T_A \le +85°C$

$+4.5V \le V_A \le +5.5V$

$+2.7V \le V_{IO} \le +5.5V$

$+0.5V \le V_{REF} \le +5.5V$

$1\ MHz \le f_{SCLK} \le 5\ MHz$

V_{CM}

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ANALOG INPUT CONSIDERATIONS

As stated previously in Section 2.6, it is not critical for the performance of the ADC161S626 to filter out the voltage spike that occurs when the ADC161S626 enters acquisition (t_{ACQ}) mode at the end of the conversion window. However, it is critical that a system designer ensures that the transients of the spike settle out within t_{ACQ}. The burden of this task can be placed on the analog source itself or the burden can be shared by the source and an external capacitor, C_{EXT} as shown in Figure 15. The external capacitor acts as a local charge reservoir for the internal sampling capacitor and thus reduces the size of the voltage spike. For low frequency analog sources such as sensors with DC-like output behaviors, C_{EXT} values greater than 1 nF are recommended. However, some sensors and signal conditioning circuitry will not be able to maintain their stability in the presence of the external capacitive load. In these instances, a series resistor (R_{EXT}) is recommended. The magnitude of R_{EXT} is dependent on the output capability of the analog source and the settling requirement of the ADC. Independent of the presence of an external capacitor, the system designer always has the option of lowering the sample rate of the ADC161S626 which directly controls the amount of time allowed for the voltage spike to settle. The slower the sample rate, the longer the t_{ACQ} time or settling time. This is possible with the ADC161S626 since the converter enters t_{ACQ} at the end of the prior conversion and thus is tracking the analog input source the entire time between conversions.

POWER CONSUMPTION

The architecture, design, and fabrication process allow the ADC161S626 to operate at conversion rates up to 250 kSPS while consuming very little power. The ADC161S626 consumes the least amount of power while operating in acquisition (power-down) mode. For applications where power consumption is critical, the ADC161S626 should be operated in acquisition mode as often as the application will tolerate. To further reduce power consumption, stop the SCLK while $\overline{CS}$ is high.

Short Cycling

Short cycling refers to the process of halting a conversion after the last needed bit is outputted. Short cycling can be used to lower the power consumption in those applications that do not need a full 16-bit resolution, or where an analog signal is being monitored until some condition occurs. In some circumstances, the conversion could be terminated after the first few bits. This will lower power consumption in the converter since the ADC161S626 spends more time in acquisition mode and less time in conversion mode.

Short cycling is accomplished by pulling $\overline{CS}$ high after the last required bit is received from the ADC161S626 output. This is possible because the ADC161S626 places the latest converted data bit on D_{OUT} as it is generated. If only 10-bits of the conversion result are needed, for example, the conversion can be terminated by pulling $\overline{CS}$ high after the 10th bit has been clocked out.

Burst Mode Operation

Normal operation of the ADC161S626 requires the SCLK frequency to be 20 times the sample rate and the $\overline{CS}$ rate to be the same as the sample rate. However, in order to minimize power consumption in applications requiring sample rates below 250 kSPS, the ADC161S626 should be run with an SCLK frequency of 5 MHz and a $\overline{CS}$ rate as slow as the system requires. When this is accomplished, the ADC161S626 is operating in burst mode. The ADC161S626 enters into acquisition mode at the end of each conversion, minimizing power consumption. This causes the converter to spend the longest possible time in acquisition mode. Since power consumption scales directly with conversion rate, minimizing power consumption requires determining the lowest conversion rate that will satisfy the requirements of the system.

PCB LAYOUT AND CIRCUIT CONSIDERATIONS

For best performance, care should be taken with the physical layout of the printed circuit board. This is especially true with a low V_{REF} or when the conversion rate is high. At high clock rates there is less time for settling, so it is important that any noise settles out before the conversion begins.

Analog and Digital Power Supplies

Any ADC architecture is sensitive to spikes on the power supply, reference, and ground pins. These spikes may originate from switching power supplies, digital logic, high power devices, and other sources. Power to the ADC161S626 should be clean and well bypassed. A 0.1 µF ceramic bypass capacitor and a 1 µF to 10 µF capacitor should be used to bypass the ADC161S626 supply, with the 0.1 µF capacitor placed as close to the ADC161S626 package as possible.

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Since the ADC161S626 has both the V_A and V_{IO} pins, the user has three options on how to connect these pins. The first option is to tie V_A and V_{IO} together and power them with the same power supply. This is the most cost effective way of powering the ADC161S626 but is also the least ideal. As stated previously, noise from V_{IO} can couple into V_A and adversely affect performance. The other two options involve the user powering V_A and V_{IO} with separate supply voltages. These supply voltages can have the same amplitude or they can be different. V_A can be set to any value between +4.5V and +5.5V; while V_{IO} can be set to any value between +2.7V and +5.5V.

Best performance will typically be achieved with V_A operating at 5V and V_{IO} at 3V. Operating V_A at 5V offers the best linearity and dynamic performance when V_{REF} is also set to 5V; while operating V_{IO} at 3V reduces the power consumption of the digital logic. Operating the digital interface at 3V also has the added benefit of decreasing the noise created by charging and discharging the capacitance of the digital interface pins.

Voltage Reference

The reference source must have a low output impedance and needs to be bypassed with a minimum capacitor value of 0.1 µF. A larger capacitor value of 1 µF to 10 µF placed in parallel with the 0.1 µF is preferred. While the ADC161S626 draws very little current from the reference on average, there are higher instantaneous current spikes at the reference.

V_{REF} of the ADC161S626, like all A/D converters, does not reject noise or voltage variations. Keep this in mind if V_{REF} is derived from the power supply. Any noise and/or ripple from the supply that is not rejected by the external reference circuitry will appear in the digital results. The use of an active reference source is recommended. The LM4040 and LM4050 shunt reference families and the LM4120 and LM4140 series reference families are excellent choices for a reference source.

PCB Layout

Capacitive coupling between the noisy digital circuitry and the sensitive analog circuitry can lead to poor performance. The solution is to keep the analog circuitry separated from the digital circuitry and the clock line as short as possible. Digital circuits create substantial supply and ground current transients. The logic noise generated could have significant impact upon system noise performance. To avoid performance degradation of the ADC161S626 due to supply noise, avoid using the same supply for the V_A and V_{REF} of the ADC161S626 that is used for digital circuitry on the board.

Generally, analog and digital lines should cross each other at 90° to avoid crosstalk. However, to maximize accuracy in high resolution systems, avoid crossing analog and digital lines altogether. It is important to keep clock lines as short as possible and isolated from ALL other lines, including other digital lines. In addition, the clock line should also be treated as a transmission line and be properly terminated. The analog input should be isolated from noisy signal traces to avoid coupling of spurious signals into the input. Any external component (e.g., a filter capacitor) connected between the converter's input pins and ground or to the reference input pin and ground should be connected to a very clean point in the ground plane.

A single, uniform ground plane and the use of split power planes are recommended. The power planes should be located within the same board layer. All analog circuitry (input amplifiers, filters, reference components, etc.) should be placed over the analog power plane. All digital circuitry should be placed over the digital power plane. Furthermore, the GND pins on the ADC161S626 and all the components in the reference circuitry and input signal chain that are connected to ground should be connected to the ground plane at a quiet point. Avoid connecting these points too close to the ground point of a microprocessor, microcontroller, digital signal processor, or other high power digital device.

APPLICATION CIRCUITS

The following figures are examples of the ADC161S626 in typical application circuits. These circuits are basic and will generally require modification for specific circumstances.

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Data Acquisition

Figure 17 shows a typical connection diagram for the ADC161S626 operating at V_A of +5V. V_{REF} is connected to a 2.5V shunt reference, the LM4020-2.5, to define the analog input range of the ADC161S626 independent of supply variation on the +5V supply line. The V_{REF} pin should be de-coupled to the ground plane by a 0.1 µF ceramic capacitor and a tantalum capacitor of 10 µF. It is important that the 0.1 µF capacitor be placed as close as possible to the V_{REF} pin while the placement of the tantalum capacitor is less critical. It is also recommended that the V_A and V_{IO} pins of the ADC161S626 be de-coupled to ground by a 0.1 µF ceramic capacitor in parallel with a 10 µF tantalum capacitor.

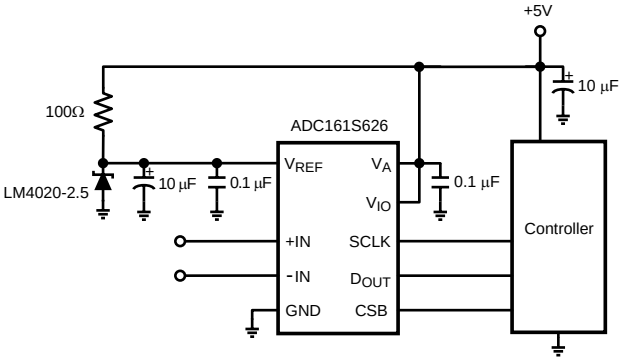

Figure 17. Low cost, low power Data Acquisition System

Bridge Sensor Application

Figure 18 and Figure 19 show examples of interfacing bridge sensors to the ADC161S626. The applications assume that the bridge sensors require buffering and amplification to fully utilize the dynamic range of the ADC and thus optimize the performance of the entire signal path. The amplification stages consist of the LMP7732 and the LMP7731, dual and single precision amplifiers, and some gain setting passive components. The amplification stages offer the benefit of high input impedance and high amplification capability.

Figure 19, which has the amplification stage configured as an instrumentation amplifier, has the added benefit of additional common-mode rejection of common-mode noise or DC-voltages coming from the bridge sensor. Depending on the voltage applied at V_{CM}, the ADC161S626 in the single-ended application will convert the output voltage of a bridge sensor that contains both a positive and negative component or a bridge sensor that only outputs a positive voltage. For the case of a sensor with both positive and negative output capability, it is recommended that V_{CM} be connected to V_{REF}. For a sensor that only outputs a positive voltage, V_{CM} would need to be connected to ground. Both of these scenarios will allow all the ADC output codes to be potentially utilized.

A separate power supply (V_{BR}) is assumed to be biasing the bridge sensor but another option for biasing the bridge sensor would be powering it from the +5V power supply. This option has the benefit of providing the ideal common-mode input voltage for the ADC161S626, while keeping design complexity and cost to a minimum. However, any fluctuation in the +5V supply will still be visible on the differential input to the amplification stage. The LM4120-4.1, a 4.1V series reference, and the LM4120-2.5, a 2.5V series reference, are used as the reference voltages in the respective application drawings. The application in Figure 19 is limited to a V_{REF} of 2.5V or less because of the single-ended configuration of the differential ADC161S626, as discussed in Section 2.2. The ADC161S626 and the LM4120's are all powered from the same +5V voltage source.

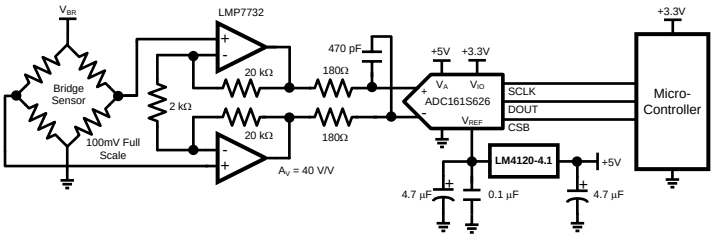

Figure 18. Differential Application for a Bridge Sensor

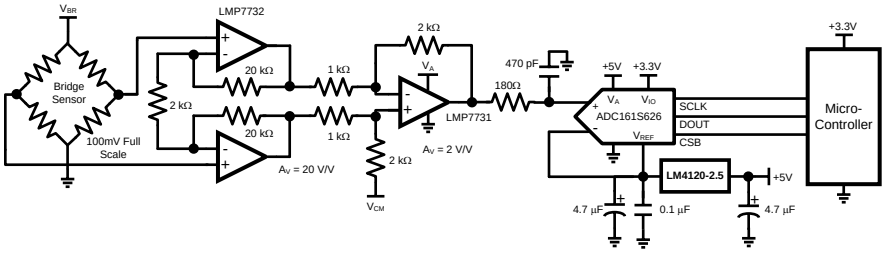

Figure 19. Single-Ended Application for a Bridge Sensor

Current Sensing Application

Figure 20 shows an example of interfacing a current transducer to the ADC161S626. The current transducer converts an input current into a voltage that is converted by the ADC. Since the output voltage of the current transducer is single-ended and centered around a common-mode voltage (V_{CM}) of 2.5V, the ADC161S626 is configured with the output of the transducer driving the non-inverting input and V_{CM} of the transducer driving the inverting input. The output of the transducer has an output range of ±2.5V around V_{CM} of 2.5V. As a result, a series reference voltage of 2.5V is connected to the ADC161S626. This will allow all of the codes of the ADC161S626 to be available for the application. This configuration of the ADC161S626 is referred to as a single-ended application of a differential ADC. All of the elements in the application are conveniently powered by the same +5V power supply, keeping circuit complexity and cost to a minimum.

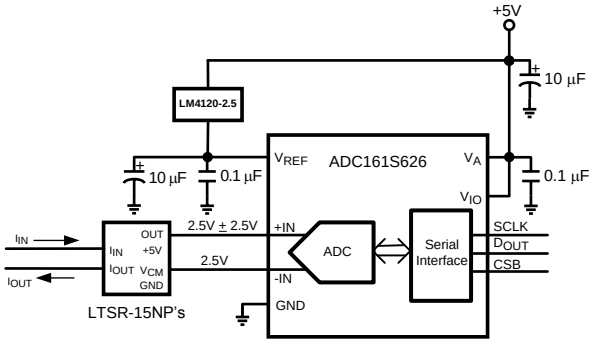

Figure 20. Interfacing the ADC161S626 to a Current Transducer

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
ADC161S626CIMM/NOPB	ACTIVE	VSSOP	DGS	10	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
ADC161S626CIMME/NOPB	ACTIVE	VSSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
ADC161S626CIMMX/NOPB	ACTIVE	VSSOP	DGS	10	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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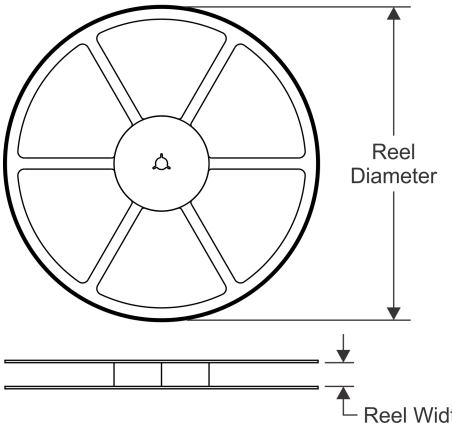
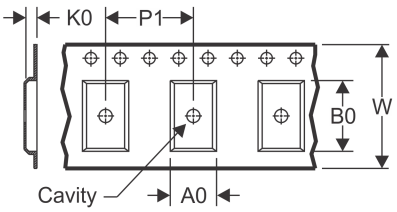
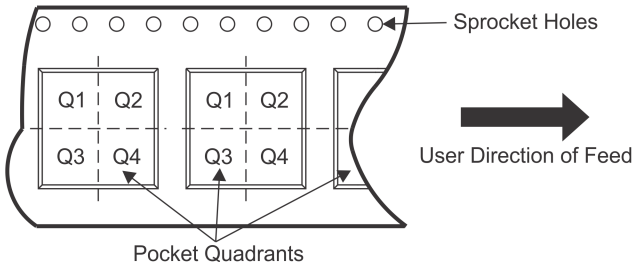


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

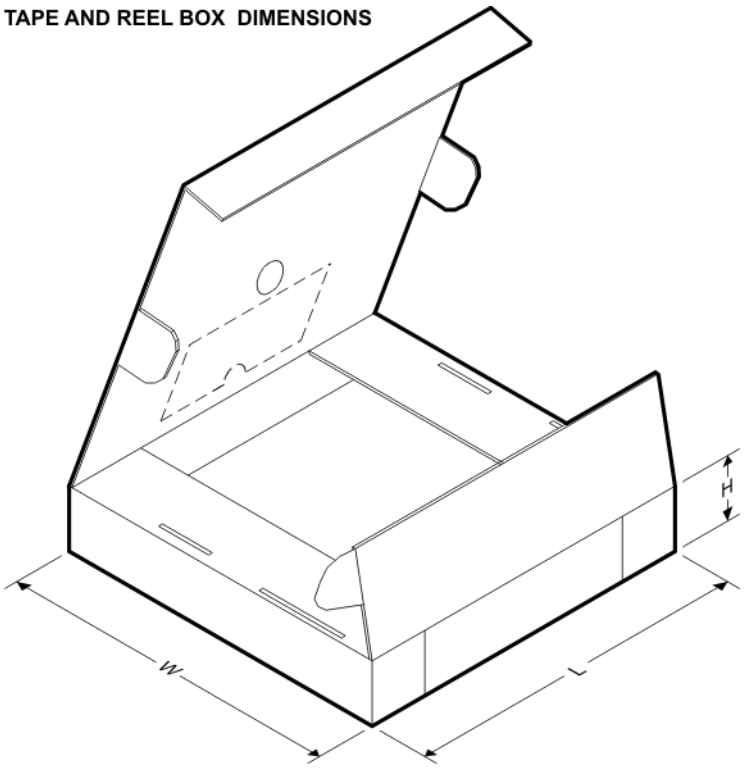
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADC161S626CIMM/NOPB	VSSOP	DGS	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
ADC161S626CIMME/NOPB	VSSOP	DGS	10	250	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
ADC161S626CIMMX/NOPB	VSSOP	DGS	10	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

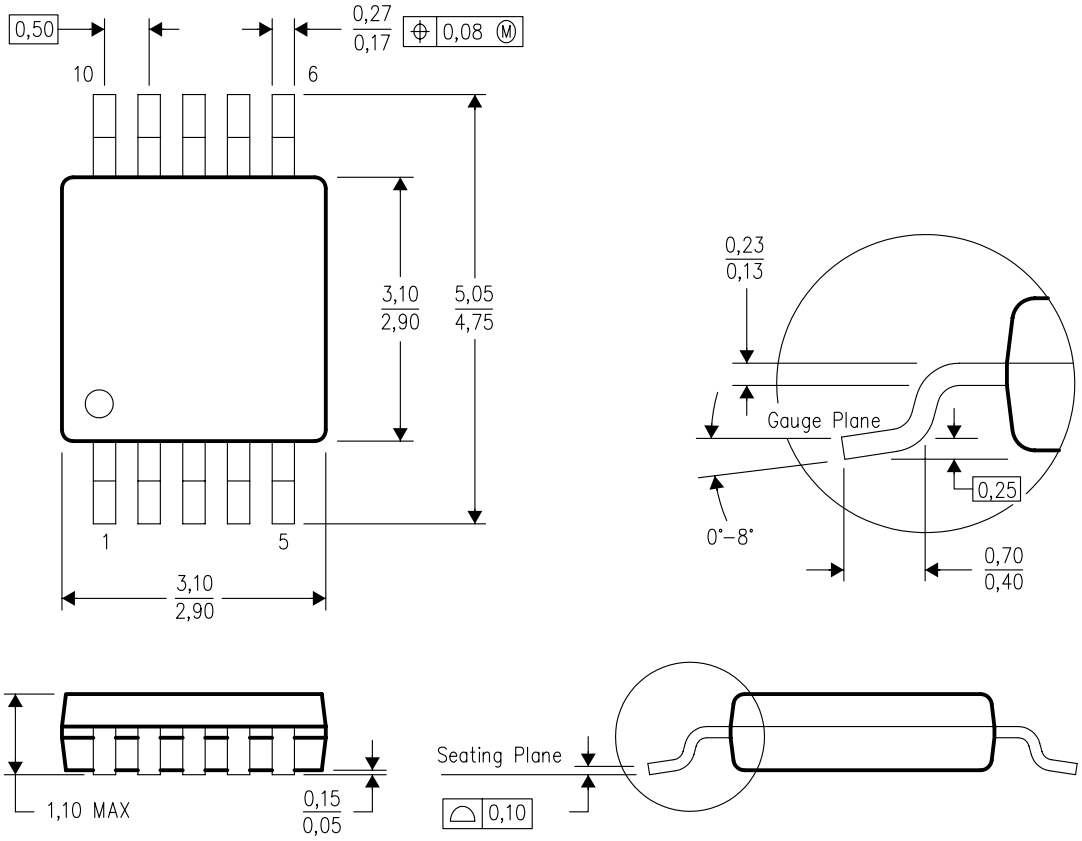
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADC161S626CIMM/NOPB	VSSOP	DGS	10	1000	203.0	190.0	41.0
ADC161S626CIMME/NOPB	VSSOP	DGS	10	250	203.0	190.0	41.0
ADC161S626CIMMX/NOPB	VSSOP	DGS	10	3500	349.0	337.0	45.0

DGS (S–PDSO–G10) PLASTIC SMALL–OUTLINE PACKAGE



4073272/C 02/04

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–187 variation BA.

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