Robust RS-485 Transceiver

Check for Samples: SN65HVD82

FEATURES

- **Bus I/O Protection**
  - **±16 kV HBM protection**
  - **±12 kV IEC61000-4-2 Contact Discharge**
  - **+4kV IEC61000-4-4 Fast Transient Burst**
- **Industrial Temperature Range –40°C to 85°C**
- **Large Receiver Hysteresis (60mV typ) for Noise Rejection**
- **Low Power Consumption**
  - **<1 µA Standby Current**
  - **<1 mA Quiescent Current**
- **Signaling Rate Optimized for 250 kbps**

APPLICATIONS

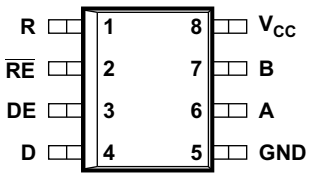
- **Electrical Meters**
- **Building Automation**
- **Industrial Networks**
- **Security Electronics**

DESCRIPTION

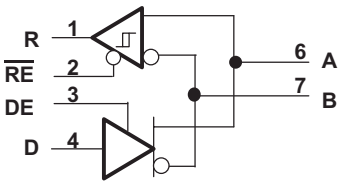
This device has robust drivers and receivers for demanding industrial applications. The bus pins are robust to ESD events, with high levels of protection to Human-Body Model, Air-Gap Discharge, and Contact Discharge specifications.

The device combines a differential driver and a differential receiver, which operate from a single 5V power supply. The driver differential outputs and the receiver differential inputs are connected internally to form a bus port suitable for half-duplex (two-wire bus) communication. The device features a wide common-mode voltage range making the device suitable for multi-point applications over long cable runs. The device is characterized from –40°C to 85°C.

(Top View)



Logic Diagram (Positive Logic)



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DRIVER FUNCTION TABLE

INPUT	ENABLE	OUTPUTS		
D	DE	A	B	
H	H	H	L	Actively drive bus High
L	H	L	H	Actively drive bus Low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drive bus High by default

RECEIVER FUNCTION TABLE

DIFFERENTIAL INPUT	ENABLE	OUTPUT	
$V_{ID} = V_A - V_B$	RE	R	
$V_{IT+} < V_{ID}$	L	H	Receive valid bus High
$V_{IT-} < V_{ID} < V_{IT+}$	L	?	Indeterminate bus state
$V_{ID} < V_{IT-}$	L	L	Receive valid bus Low
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled by default
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	Fail-safe high output
Idle (terminated) bus	L	H	Fail-safe high output

ABSOLUTE MAXIMUM RATINGS(1)

		VALUE		UNIT
		MIN	MAX	
V_{CC}	Supply voltage	–0.5	7	V
	Voltage range at A or B Inputs	–18	18	V
	Input voltage range at any logic pin	–0.3	5.7	V
	Voltage input range, transient pulse, A and B, through 100Ω	–100	100	V
	Receiver output current	–24	24	mA
T_J	Junction temperature		170	°C
T_{STG}	Storage temperature	–65	150	°C
	Continuous total power dissipation	See Thermal Table		
	IEC 61000-4-2 ESD (Contact Discharge), bus terminals and GND		±12	kV
	IEC 60749-26 ESD (Human Body Model), bus terminals and GND		±16	kV
	IEC 61000-4-4 EMC (Fast Transient Burst Immunity), bus terminals and GND		±4	kV
	JEDEC Standard 22, Test Method A114 (Human Body Model), all pins		±4	kV
	JEDEC Standard 22, Test Method C101 (Charged Device Model), all pins		±1.5	kV
	JEDEC Standard 22, Test Method A115 (Machine Model), all pins		±100	V

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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THERMAL INFORMATION

THERMAL METRIC(1)		SN65HVD82 PACKAGE SOIC (D)	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	116.1	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	60.8	
θ_{JB}	Junction-to-board thermal resistance(2)	57.1	
ψ_{JT}	Junction-to-top characterization parameter	13.9	
ψ_{JB}	Junction-to-board characterization parameter	56.5	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	NA	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_I	Input voltage at any bus terminal (separately or common mode)(1)	–7		12	V
V_{IH}	High-level input voltage (D, DE and $\overline{RE}$ inputs)	2		VCC	V
V_{IL}	Low-level input voltage (D, DE and $\overline{RE}$ inputs)	0		0.8	V
V_{ID}	Differential input voltage (A and B inputs)	–12		12	V
I_O	Output current, Driver	–60		60	mA
	Output current, Receiver	–8		8	mA
R_L	Differential load resistance	54	60		Ω
C_L	Differential load capacitance		50		pF
$1/t_{UI}$	Signaling rate			250	kbps
T_A	Operating free-air temperature (see application section for thermal information)	–40		85	°C
T_J	Junction Temperature	–40		150	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

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ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$\|V_{OD}\|$	Driver differential output voltage magnitude	See Figure 1, R_L = 60 Ω, 375 Ω on each output to –7 V to 12 V		1.5			V
		R_L = 54 Ω (RS-485)	See Figure 2	1.5	2		V
		R_L = 100 Ω (RS-422)		2	2.5		V
$\Delta\|V_{OD}\|$	Change in magnitude of driver differential output voltage	R_L = 54 Ω, C_L = 50 pF		–0.2	0	0.2	V
$V_{OC(SS)}$	Steady-state common-mode output voltage	Center of two 27-Ω load resistors		1	V_{CC}/2	3	V
ΔV_{OC}	Change in differential driver output common-mode voltage			–0.2	0	0.2	V
$V_{OC(PP)}$	Peak-to-peak driver common-mode output voltage				850		mV
C_{OD}	Differential output capacitance				8		pF
V_{IT+}	Positive-going receiver differential input voltage threshold			See (1)	–70	-20	mV
$V_{IT–}$	Negative-going receiver differential input voltage threshold			–200	–150	See (1)	mV
V_{HYS}	Receiver differential input voltage threshold hysteresis ($V_{IT+} – V_{IT–}$)			40	60		mV
V_{OH}	Receiver high-level output voltage	I_{OH} = -8 mA		2.4	V_{CC}–0.3		V
V_{OL}	Receiver low-level output voltage	I_{OL} = 8 mA			0.2	0.4	V
I_I	Driver input, driver enable, and receiver enable input current			–2		2	µA
I_{OZ}	Receiver output high-impedance current	V_O = 0 V or V_{CC}, $\overline{RE}$ at V_{CC}		–10		10	µA
I_{OS}	Driver short-circuit output current	$\|I_{OS}\|$ with V_A or V_B from –7 V to +12 V				150	mA
I_I	Bus input current (disabled driver)	V_{CC} = 4.5 to 5.5 V or V_{CC} = 0 V, DE at 0 V	V_I = 12 V		75	125	µA
			V_I = –7 V	–100	–40		
I_{CC}	Supply current (quiescent)	Driver and Receiver enabled	DE = V_{CC}, RE=GND, No load			900	µA
		Driver enabled, receiver disabled	DE = V_{CC}, RE = V_{CC}, No load			650	
		Driver disabled, receiver enabled	DE = GND, RE = GND, No load			650	
		Driver and receiver disabled	DE = GND, D=GND, RE = V_{CC}, No load		0.4	2	
	Supply current (dynamic)	See “TYPICAL CHARACTERISTICS” section					

(1) Under any specific conditions, V_{IT+} is assured to be at least V_{HYS} higher than V_{IT-}.

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SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DRIVER							
t_r, t_f	Driver differential output rise/fall time	R_L = 54 Ω, C_L = 50 pF, See Figure 3		400	700	1200	ns
t_{PHL}, t_{PLH}	Driver propagation delay			90	700	1000	ns
$t_{SK(P)}$	Driver pulse skew, $\|t_{PHL} - t_{PLH}\|$				25	200	ns
t_{PHZ}, t_{PLZ}	Driver disable time		See Figure 4 and Figure 5		50	500	ns
t_{PZH}, t_{PZL}	Driver enable time	Receiver enabled			500	1000	ns
		Receiver disabled			3	9	µs
RECEIVER							
t_r, t_f	Receiver output rise/fall time	C_L = 15 pF, See Figure 6			18	30	ns
t_{PHL}, t_{PLH}	Receiver propagation delay time				85	195	ns
$t_{SK(P)}$	Receiver pulse skew, $\|t_{PHL} - t_{PLH}\|$				1	15	ns
t_{PLZ}, t_{PHZ}	Receiver disable time				50	500	ns
$t_{PZL(1)}$, $t_{PZH(1)}$	Receiver enable time	Driver enabled, See Figure 7			20	130	ns
$t_{PZL(2)}$, $t_{PZH(2)}$		Driver disabled, See Figure 8			2	8	µs

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PARAMETER MEASUREMENT INFORMATION

Input generator rate is 100 kbps, 50% duty cycle, rise and fall times less than 6 nsec, output impedance 50 Ω.

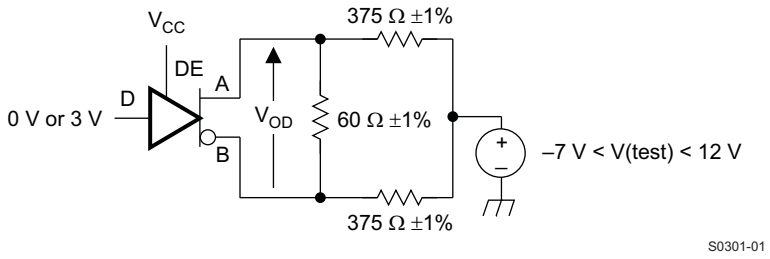


Figure 1. Measurement of Driver Differential Output Voltage With Common-Mode Load

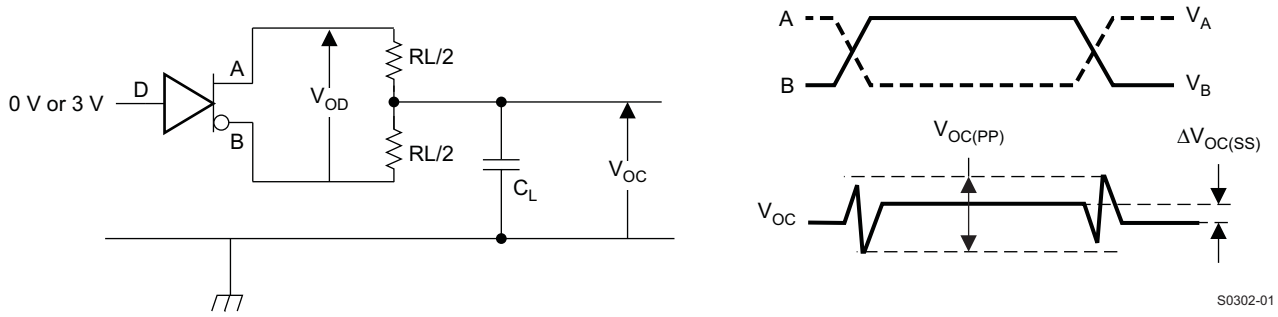


Figure 2. Measurement of Driver Differential and Common-Mode Output With RS-485 Load

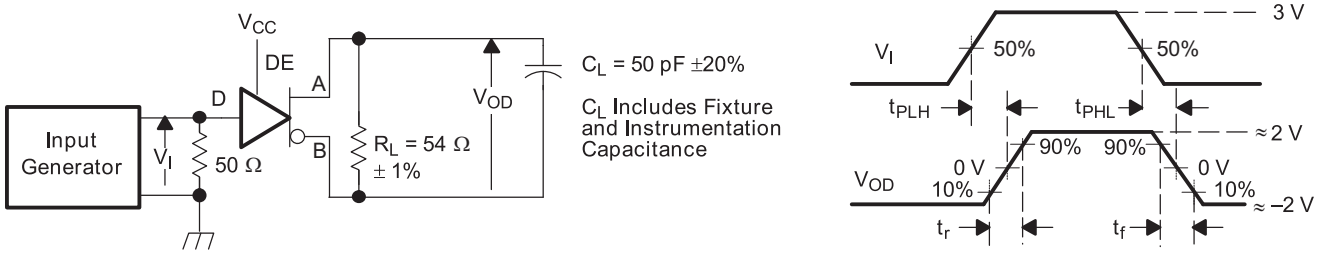
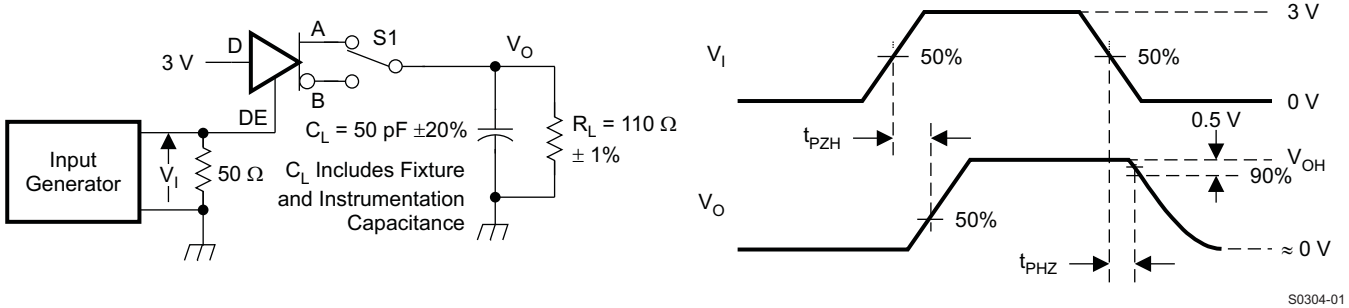


Figure 3. Measurement of Driver Differential Output Rise and Fall Times and Propagation Delays



D at 3V to test non-inverting output, D at 0V to test inverting output.

Figure 4. Measurement of Driver Enable and Disable Times With Active High Output and Pull-Down Load

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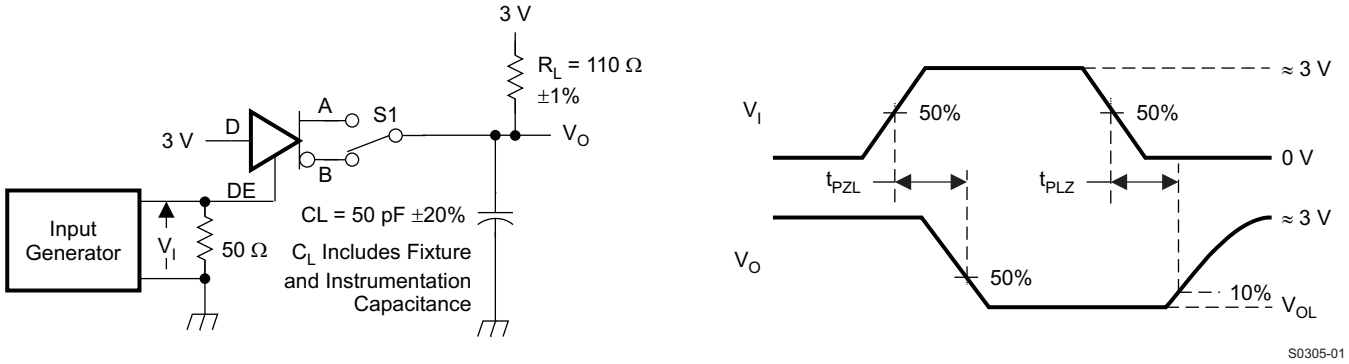
PARAMETER MEASUREMENT INFORMATION (continued)



D at 0V to test non-inverting output, D at 3V to test inverting output.

Figure 5. Measurement of Driver Enable and Disable Times With Active Low Output and Pull-up Load

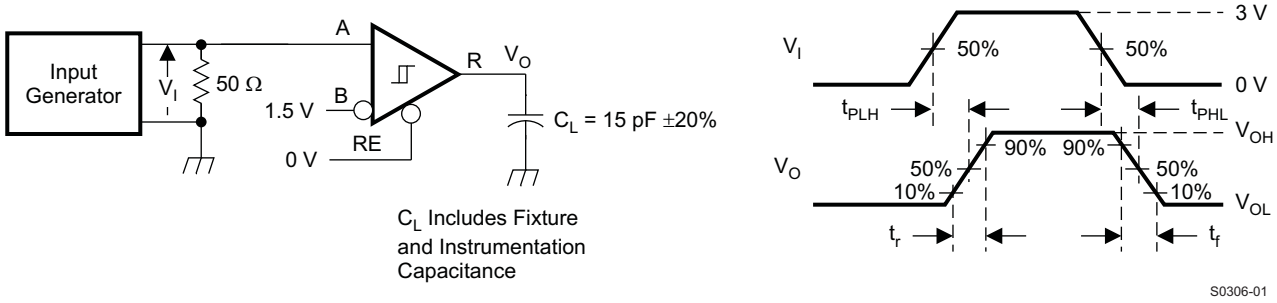


Figure 6. Measurement of Receiver Output Rise and Fall Times and Propagation Delays

PARAMETER MEASUREMENT INFORMATION (continued)

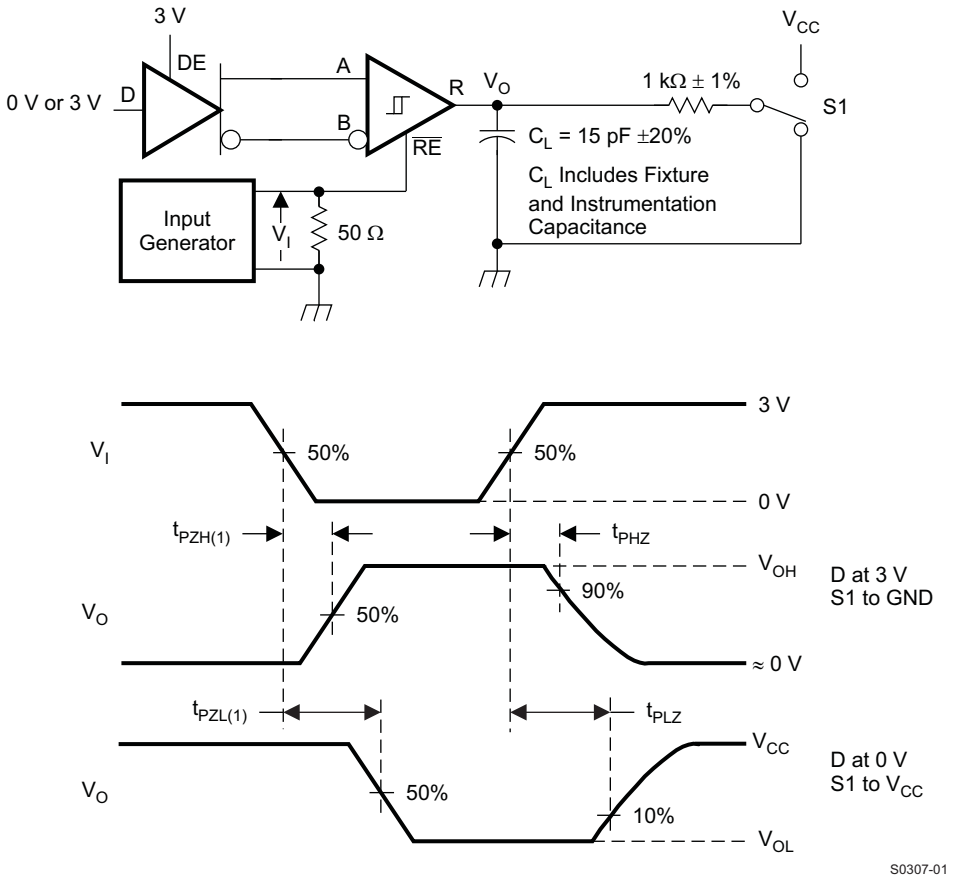


Figure 7. Measurement of Receiver Enable/Disable Times With Driver Enabled

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PARAMETER MEASUREMENT INFORMATION (continued)

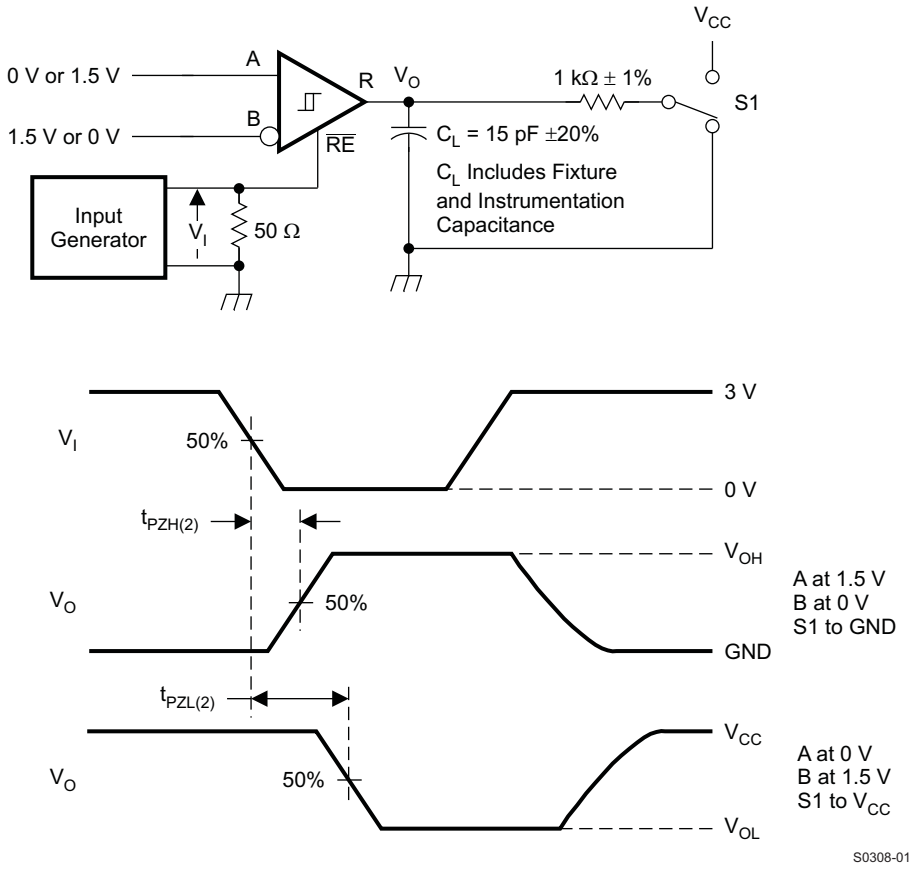
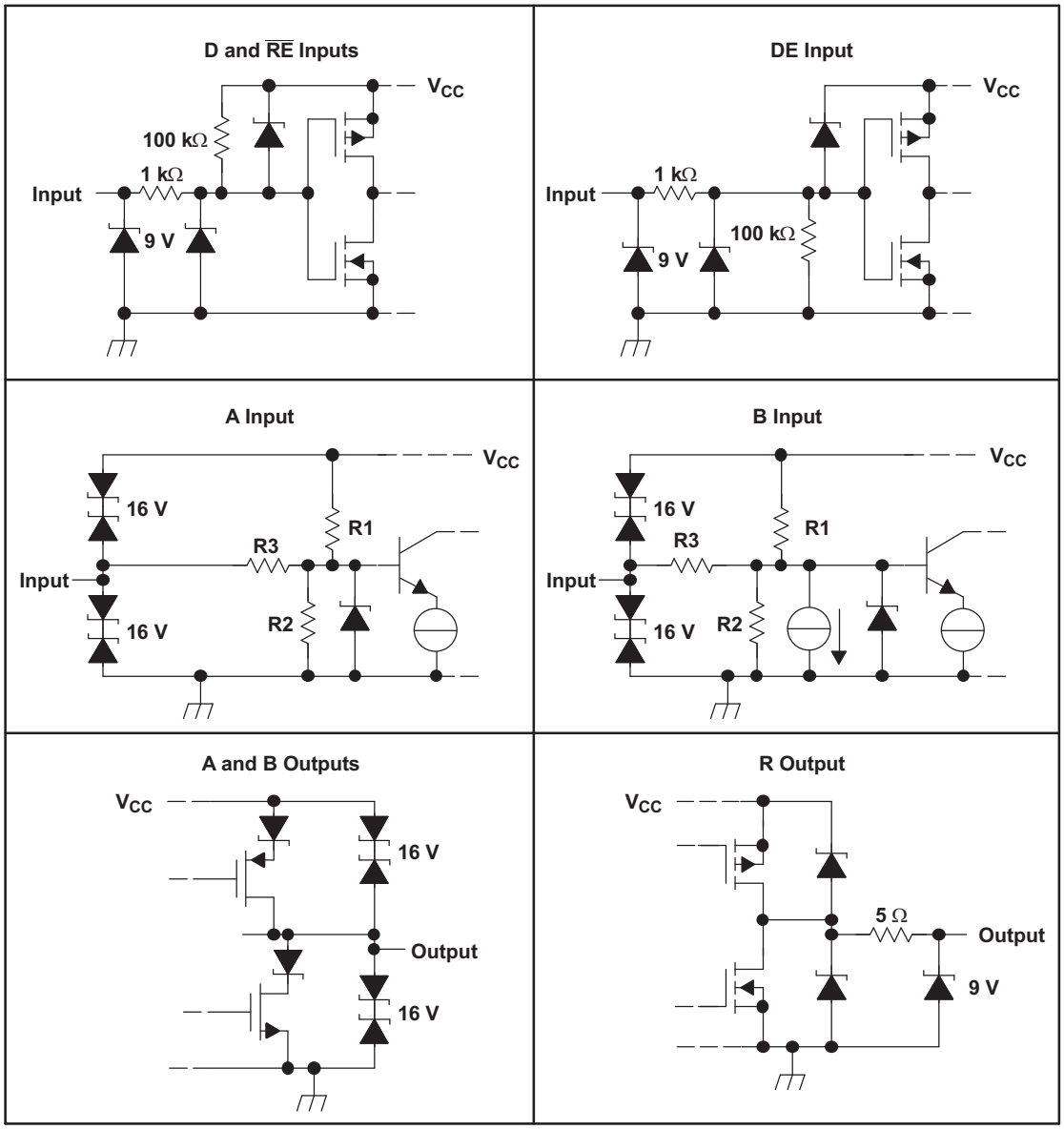


Figure 8. Measurement of Receiver Enable Times With Driver Disabled

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



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TYPICAL CHARACTERISTICS

DRIVER OUTPUT VOLTAGE vs DRIVER OUTPUT CURRENT

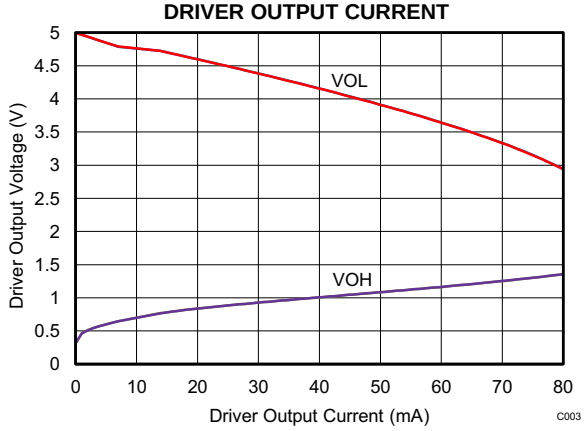

Figure 9.

DRIVER RISE AND FALL TIME vs TEMPERATURE

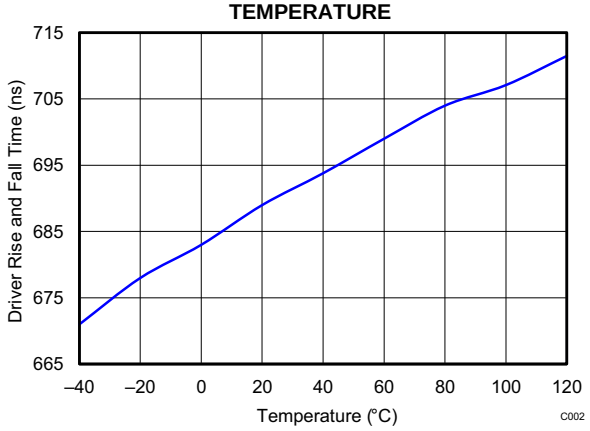

Figure 10.

SUPPLY CURRENT vs SIGNALING RATE

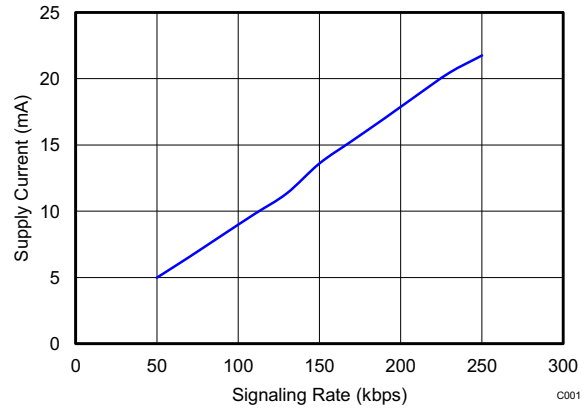

Figure 11.

RECEIVER OUTPUT vs DIFFERENTIAL INPUT VOLTAGE

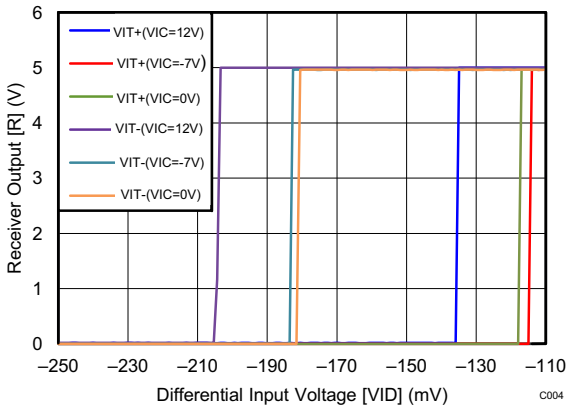

Figure 12.

DEVICE INFORMATION

Receiver Failsafe

The differential receiver is “failsafe” to invalid bus states caused by:

- open bus conditions such as a disconnected connector
- shorted bus conditions such as cable damage shorting the twisted-pair together, or
- idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the differential receiver will output a failsafe logic High state so that the output of the receiver is not indeterminate.

Receiver failsafe is accomplished by offsetting the receiver thresholds so that the “input indeterminate” range does not include zero volts differential. In order to comply with the RS-422 and RS-485 standards, the receiver output must output a High when the differential input V_{ID} is more positive than +200 mV, and must output a Low when the V_{ID} is more negative than -200 mV. The receiver parameters which determine the failsafe performance are V_{IT+} and $V_{IT-}$and V_{HYS}. As seen in the Electrical Characteristics table, differential signals more negative than -200 mV will always cause a Low receiver output. Similarly, differential signals more positive than +200 mV will always cause a High receiver output.

When the differential input signal is close to zero, it will still be above the V_{IT+} threshold, and the receiver output will be High. Only when the differential input is more negative than V_{IT-}will the receiver output transition to a Low state. So the noise immunity of the receiver inputs during a bus fault condition includes the receiver hysteresis value V_{HYS} (the separation between V_{IT+} and V_{IT-}) as well as the value of V_{IT+}.

Signals which transition from positive to negative (or from negative to positive) will transition only once, ensuring no spurious bits.

Low-Power Standby Mode

When both the driver and receiver are disabled (DE transitions to a low state and RE transitions to a high state) the device enters standby mode. If the enable inputs are in this state for a brief time (e.g. less than 100 ns), the device does not enter standby mode. This prevents inadvertently entering standby mode during driver/receiver enabling. Only when the enable inputs are held in this state a sufficient duration (e.g. for 300 ns or more), the device is assured to be in standby mode. In this low-power standby mode, most internal circuitry is powered down, and the steady-state supply current is typically less than 400 nA. When either the driver or the receiver is re-enabled, the internal circuitry becomes active.

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APPLICATION INFORMATION

DEVICE CONFIGURATION

The SN65HVD82 is a half-duplex, 250 kbps, RS-485 transceiver operating from a single 5V supply. The driver and receiver enable pins allow for the configuration of different operating modes.

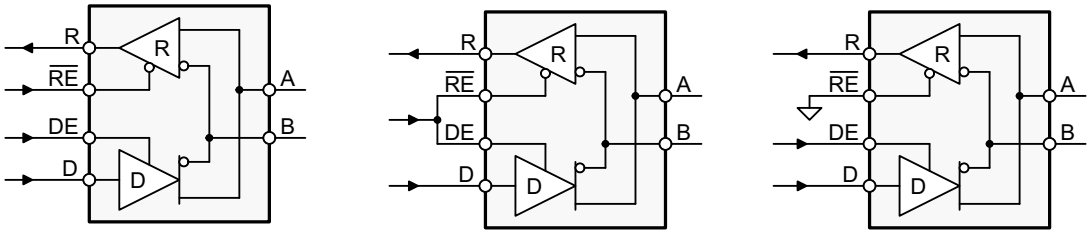

Figure 13. SN65HVD82 Transceiver Configurations

Using independent enable lines provides the most flexible control as it allows for the driver and the receiver to be turned on and off individually. While this configuration requires two control lines, it allows for selective listening into the bus traffic, whether the driver is transmitting data or not.

Combining the enable signals simplifies the interface to the controller by forming a single, direction-control signal. Thus, when the direction- control line is high, the transceiver is configured as a driver, while for a low the device operates as a receiver.

Tying the receiver-enable to ground and controlling only the driver-enable input, also uses one control line only. In this configuration a node not only receives the data from the bus but also the data it sends and thus can verify that the correct data have been transmitted.

BUS – DESIGN

An RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor, R_T, whose value matches the characteristic impedance, Z_0, of the cable. This method, known as parallel termination, allows for higher data rates over longer cable length.

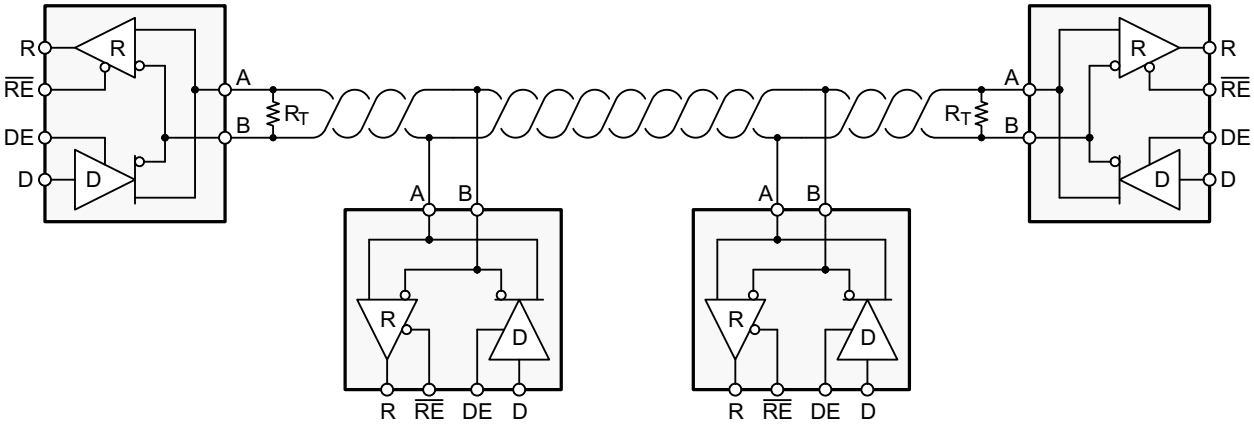

Figure 14. Typical RS-485 Network with SN65HVD82 Transceivers

Common cables used are unshielded twisted pair (UTP), such as low-cost CAT-5 cable with Z_0 = 100 Ω, and proper RS-485 cable with Z_0 = 120 Ω.

Line measurements have shown that making R_T by up to 10% larger than Z_0 improves signal quality. Typical cable sizes are AWG 22 and AWG 24.

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The theoretical maximum bus length is assumed with 4000 ft or 1200 m, and represents the length of an AWG 24 cable whose cable resistance approaches the value of the termination resistance, thus reducing the bus signal by half or 6 dB.

The theoretical maximum number of bus nodes is determined by the ratio of the RS-485 specified maximum of 32 unit loads (UL) and the actual unit load of the applied transceiver. For example, the SN65HVD82 is a 1/8 UL transceiver. Dividing 32 UL by 1/8 UL yields 256 transceivers that can be connected to one bus.

CABLE-LENGTH VERSUS DATA RATE

There is an inverse relationship between data rate and cable length. That is, the higher the data rate the shorter the cable and conversely the lower the data rate the longer the cable. While most RS-485 systems utilize data rates between 10 kbps and 100 kbps, applications such as e-metering often operate at rates of up to 250 kbps even at distances of 4000 ft and above. This is possible by allowing for small signal jitter of up to 5 or 10%.

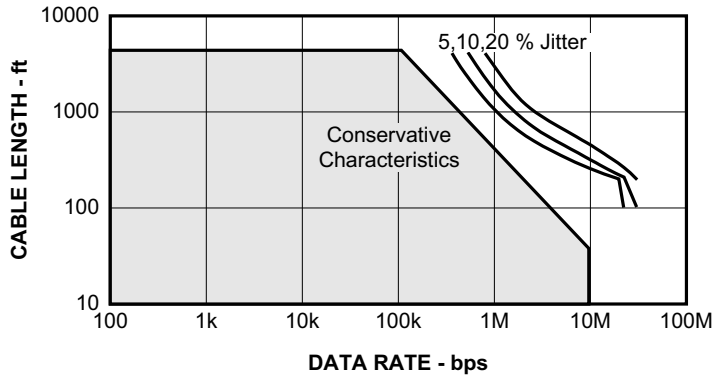

Figure 15. Cable Length vs Data Rate Characteristic

STUB – LENGTH

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, should be as short as possible. The reason for this is that a stub presents a non-terminated piece of bus line which can introduce reflections if too long. As a rule of thumb the electrical length or round-trip delay of a stub should be less than one tenth of the driver's rise time, thus leading to a maximum physical stub length of: $L_{Stub} \leq 0.1 \times t_r \times v \times c$, with $\mathbf{t}_r$ as the driver's 10/90 rise time, **c** as the speed of light (3×10^8 m/s or 9.8×10^8 ft/s), and **v** as the signal velocity of the cable (v = 78%) or trace (v = 45%) as a factor of **c**.

Thus, for the SN65HVD82 with a minimum rise time of 400 ns the maximum *cable* stub length yields $L_{Stub} \leq 0.1 \times 400 \times 10^{-9} \times 3\ 10^8 \times 0.78 = 9.4$ m or 30.6 ft.

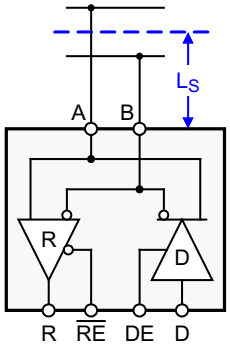

Figure 16. Stub Length

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3V–5V INTERFACE

Interfacing the SN65HVD82 to a 3V controller is easy. Because the 5V logic inputs of the transceiver accept 3V input signals they can be directly connected to the controller I/O. The 5V receiver output, R, however must be level-shifted via a Schottky diode and a 10k resistor to connect to the controller input. When R is high, the diode is reverse biased and the controller supply potential lies at the controller input. When R is low, the diode is forward biased and conducts. In this case only the diode forward voltage of 0.2V lies at the controller input.

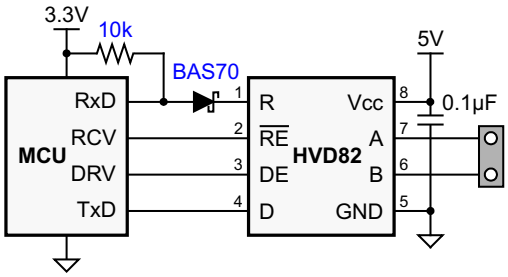

Figure 17. 3V–5V Interface

NOISE IMMUNITY

The input sensitivity of a standard RS-485 transceiver is ±200 mV. When the differential input voltage, V_{ID}, is greater than +200 mV, the receiver output turns high, for V_{ID} ≤ 200 mV the receiver outputs low. Bus voltages in between these levels can cause the receiver output to go high, or low, or even toggle between logic states. Small bus voltages however occur every time during the bus access hand-off from one driver to the next as the low-impedance termination resistors reduce the bus voltage to zero. To prevent receiver output toggling during bus idling, and thus increasing noise immunity, external bias resistors must be applied to create a bus voltage that is greater than the input sensitivity plus any expected differential noise.

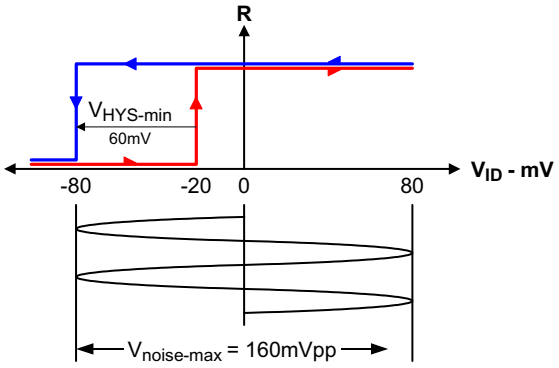

Figure 18. SN65HVD82 Noise Immunity

The SN65HVD82 transceiver circumvents idle-bus and differential noise issues by providing a positive input threshold of –20 mV and a typical hysteresis of 60 mV. In the case of an idle-bus condition therefore, a differential noise voltage of up to 160 mV_{PP} can be present without causing the receiver output to change states from high to low. This increased noise immunity eliminates the need for idle-bus failsafe bias resistors and allows for long haul data transmissions in noisy environment.

TRANSIENT PROTECTION

The bus terminals of the SN65HVD82 transceiver family possess on-chip ESD protection against ±15 kV human body model (HBM) and ±12 kV IEC61000-4-2 contact discharge. As stated in the IEC 61000-4-2 standard, contact discharge is the preferred test method; although IEC air-gap testing is less repeatable than contact testing, air discharge protection levels are inferred from the contact discharge test results. The IEC-ESD test is far more severe than the HBM-ESD test. The 50% higher charge capacitance, CS, and 78% lower discharge resistance, RD of the IEC-model produce significantly higher discharge currents than the HBM-model.

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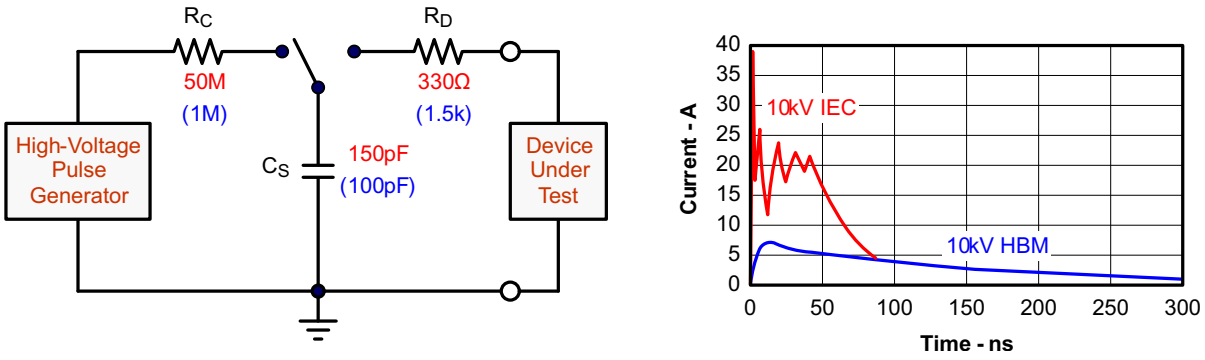

Figure 19. HBM and IEC-ESD Models and Currents in Comparison

EFTs are usually caused by relay contact bounce or the interruption of inductive loads, while surge transients often results from lightning strikes (direct strike or induced voltages and currents due to an indirect strike), or the switching of power systems including load changes and short circuits switching. These transients are often encountered in industrial environments, such as factory automation and power-grid systems.

Figure 20 compares the pulse-power of the EFT and surge transients with the power caused by an IEC-ESD transient. As can be seen the tiny blue blip in the bottom left corner of the left diagram represents the power of a 10 kV ESD transient, which already dwarfs against the significantly higher EFT power spike and certainly against the 500 V surge transient. This type of transient power is well representative for factory environments in industrial and process automation. The right diagram compares the enormous power of a 6kV surge transient, which more likely occurs in e-metering applications of power generating and power grid systems, with the aforementioned 500 V surge transient. *Note that the unit of the pulse-power changes from kW to MW, thus making the power of the 500 V surge transient almost dropping off the scale.*

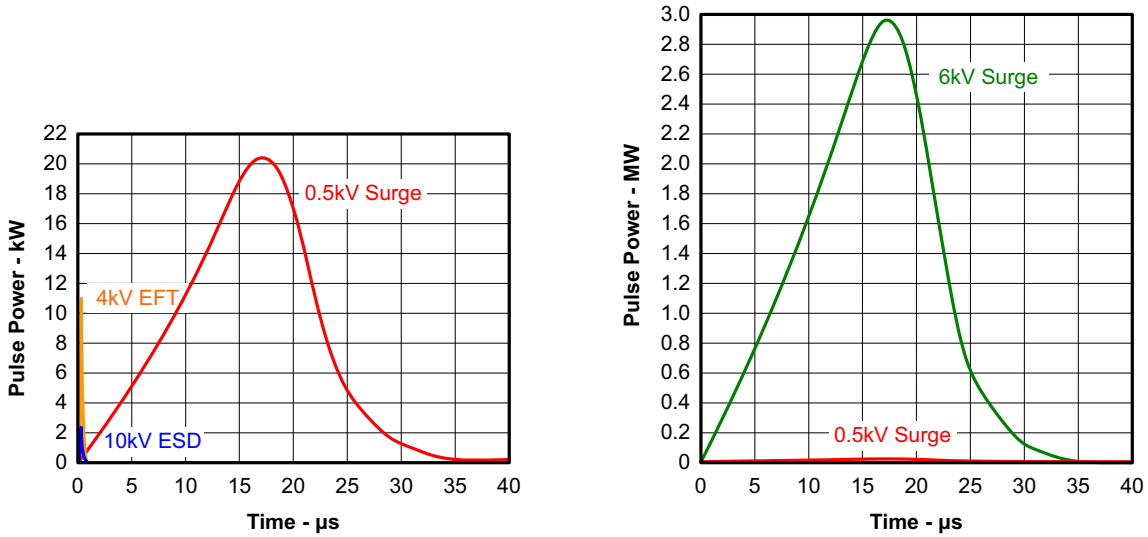

Figure 20. Power Comparison of ESD, EFT, and Surge Transients

In the case of surge transients, their long pulse duration and slowly decreasing pulse power signifies high energy content.

The electrical energy of a transient that is dumped onto the transceiver's internal protections cells is converted into thermal energy, or heat that literally fries the protection cells, thus destroying the transceiver. Figure 21 showcases the large differences in transient energies for single ESD, EFT, and surge transients as well as for an EFT pulse train, commonly applied during compliance testing.

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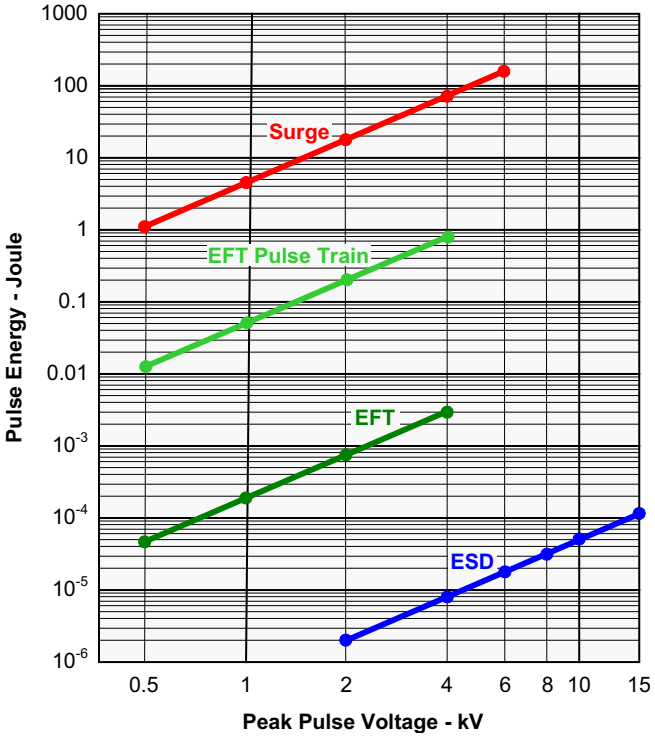

Figure 21. Comparison of Transient Energies

Figure 22 suggests two circuit designs providing protection against surge transients. Table 1 presents the associated bill of material.

Table 1. Bill of Materials

Device	Function	Order Number	Manufacturer
XCVR	3.3V, 250kbps RS-485 Transceiver	SN65HVD82D	TI
R1,R2	10Ω, Pulse-Proof Thick-Film Resistor	CRCW0603010RJNEAHP	Vishay
TVS	Bidirectional 400W Transient Suppressor	CDSOT23-SM712	Bourns
TBU1,TBU2	Bidirectional. 200mA Transient Blocking Unit	TBU-CA-065-200-WH	Bourns
MOV1,MOV2	200V, Metal-Oxide Varistor	MOV-10D201K	Bourns

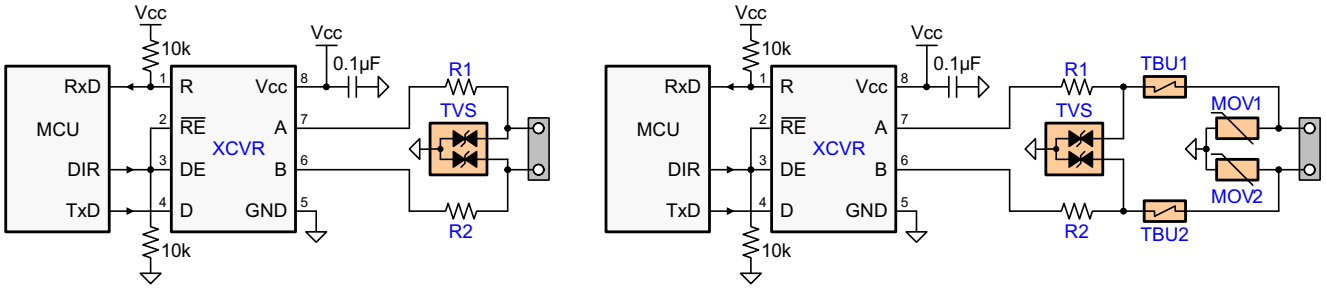

Figure 22. Transient Protection Against ESD, EFT, and Surge Transients

Both circuits are designed for 10 kV ESD and 4 kV EFT transient protection. The left however provides surge protection of ≥ 500 V transients only, while the right protection circuits can withstand surge transients of 5 kV.

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DESIGN AND LAYOUT CONSIDERATIONS FOR TRANSIENT PROTECTION

On-chip IEC-ESD protection is good for laboratory and portable equipment but never sufficient for EFT and surge transients occurring in industrial environments. Therefore robust and reliable bus node design requires the use of external transient protection devices.

Because ESD and EFT transients have a wide frequency bandwidth from approximately 3 MHz to 3 GHz, high-frequency layout techniques must be applied during PCB design.

In order for your PCB design to be successful start with the design of the protection circuit in mind.

1. Place the protection circuitry close to the bus connector to prevent noise transients from penetrating your board.
2. Use Vcc and ground planes to provide low-inductance. Note that high-frequency currents follow the path of least inductance and not the path of least impedance.
3. Design the protection components into the direction of the signal path. Do not force the transients currents to divert from the signal path to reach the protection device.
4. Apply 100 nF to 220 nF bypass capacitors as close as possible to the Vcc-pins of transceiver, UART, controller ICs on the board.
5. Use at least two vias for Vcc and ground connections of bypass capacitors and protection devices to minimize effective via-inductance.
6. Use 1k to 10k pull-up/down resistors for enable lines to limit noise currents in theses lines during transient events.
7. Insert pulse-proof resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus terminals. These resistors limit the residual clamping current into the transceiver and prevent it from latching up.
8. While pure TVS protection is sufficient for surge transients up to 1kV, higher transients require metal-oxide varistors (MOVs) which reduce the transients to a few hundred volts of clamping voltage, and transient blocking units (TBUs) that limit transient current to some 200 mA.

ISOLATED BUS NODE DESIGN

Many RS-485 networks use isolated bus nodes to prevent the creation of unintended ground loops and their disruptive impact on signal integrity. An isolated bus node typically includes a micro controller that connects to the bus transceiver via a multi-channel, digital isolator (Figure 23).

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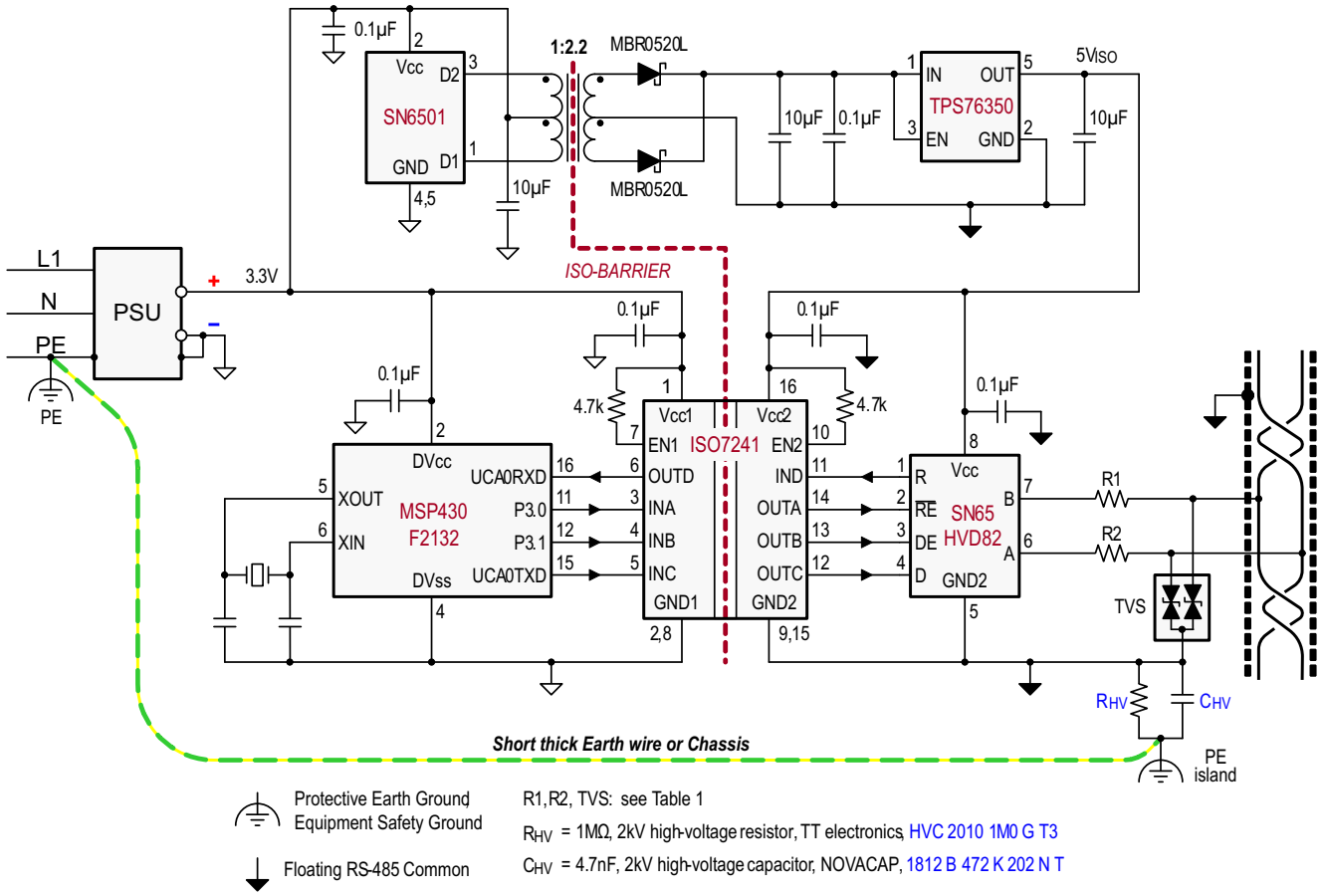

Figure 23. Isolated Bus Node With Transient Protection

Power isolation is accomplished using the push-pull transformer driver SN6501 and a low-cost LDO, TPS76350

Signal isolation utilizes the quadruple digital isolator ISO7241. Notice that both enable inputs, EN1 and EN2, are pulled-up via 4.7k resistors to limit their input currents during transient events.

While the transient protection is similar to the one in Figure 22 (left circuit), an additional high-voltage capacitor is used to divert transient energy from the floating RS-485 common further towards Protective Earth (PE) ground. This is necessary as noise transients on the bus are usually referred to Earth potential.

R_{VH} refers to a high-voltage resistor, and in some applications even a varistor. This resistance is applied to prevent charging of the floating ground to dangerous potentials during normal operation.

Occasionally varistors are used instead of resistors in order to rapidly discharge C_{HV}, if it is expected that fast transients might charge C_{HV} to high-potentials.

Note that the PE island represents a copper island on the PCB for the provision of a short, thick Earth wire connecting this island to PE ground at the entrance of the power supply unit (PSU).

In equipment designs using a chassis, the PE connection is usually provided through the chassis itself. Typically the PE conductor is tied to the chassis at one end while the high-voltage components, C_{HV} and R_{HV}, are connecting to the chassis at the other end.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN65HVD82D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HVD82	Samples
SN65HVD82DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HVD82	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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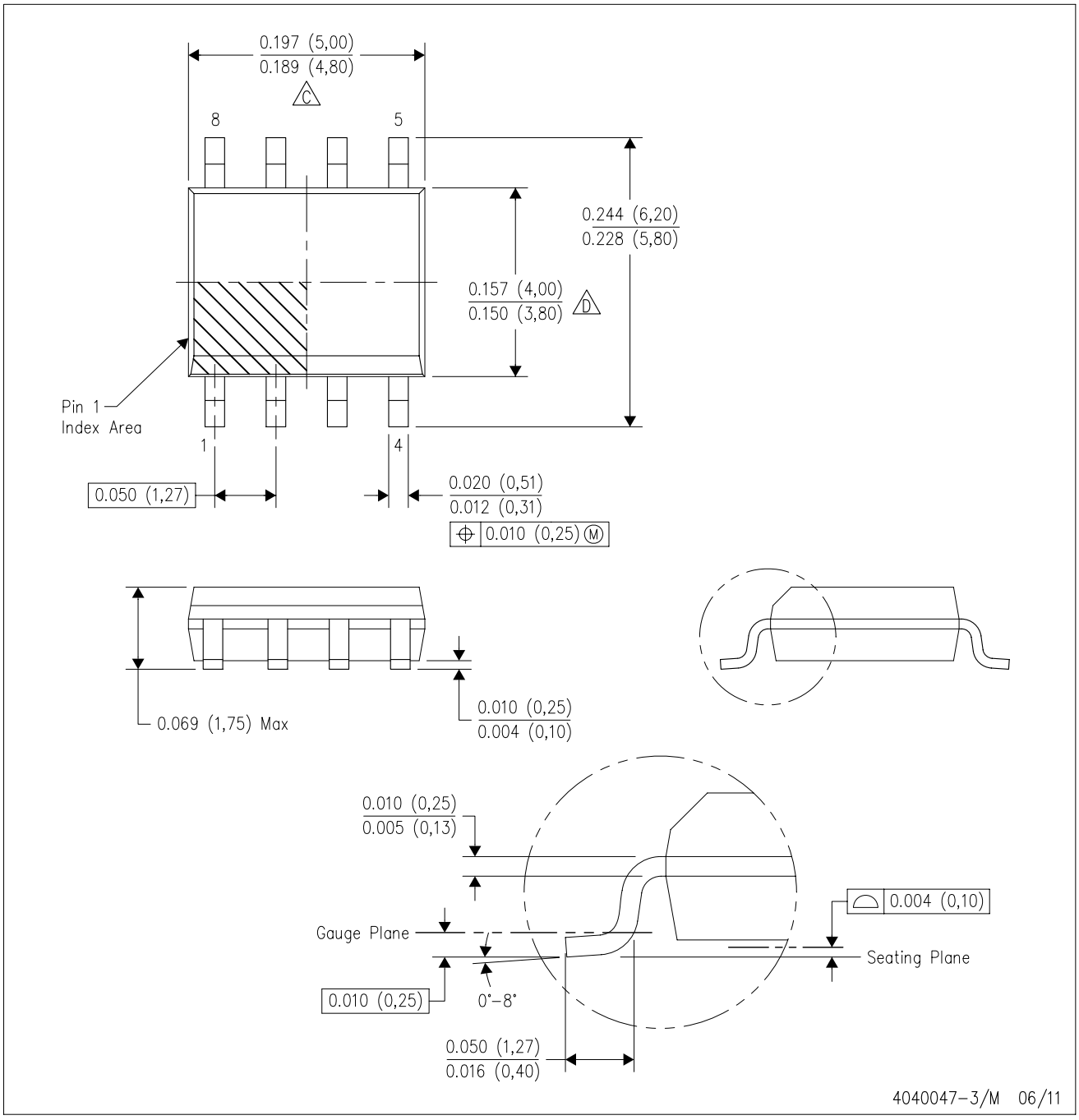

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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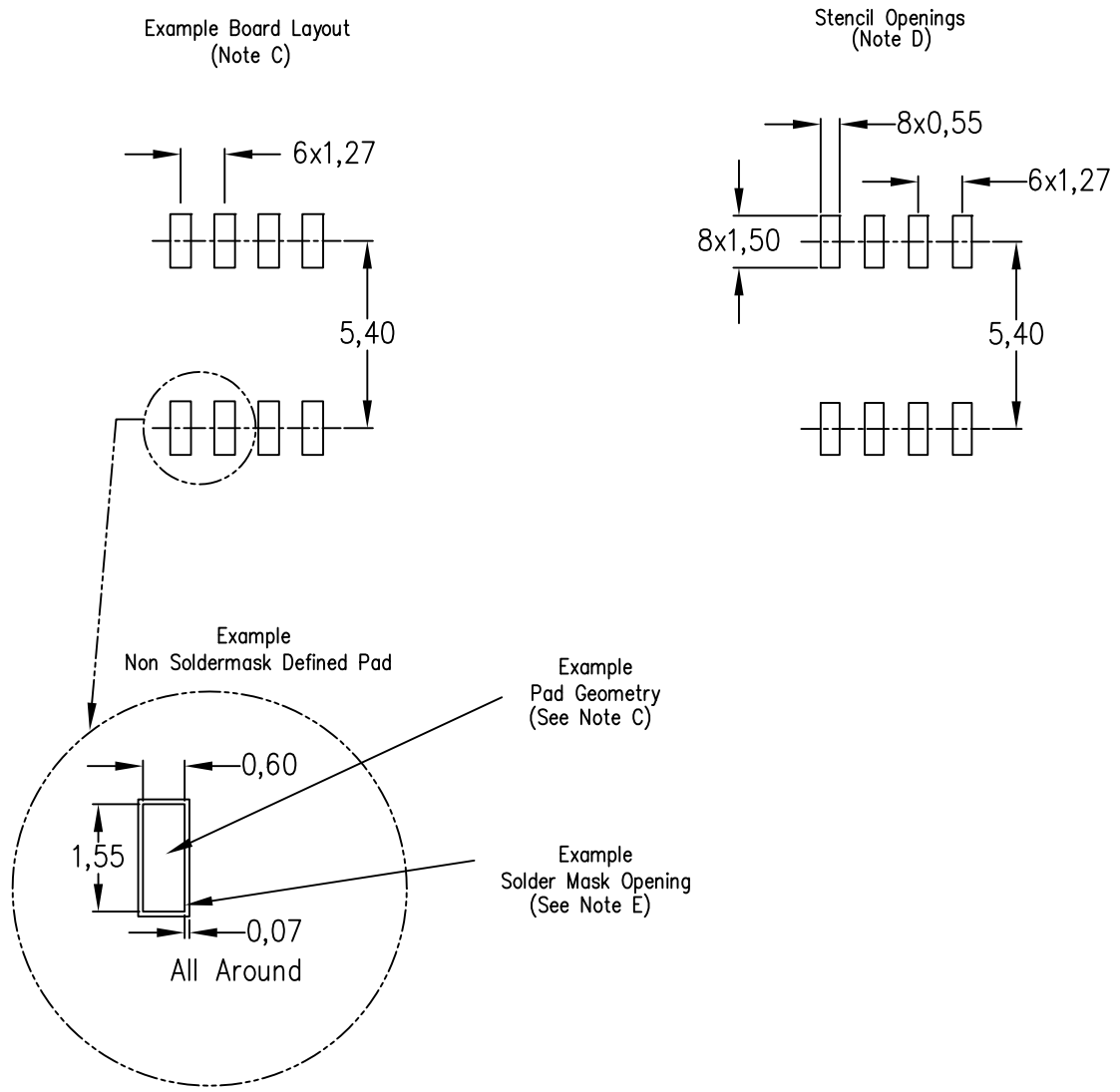

NOTES:
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B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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