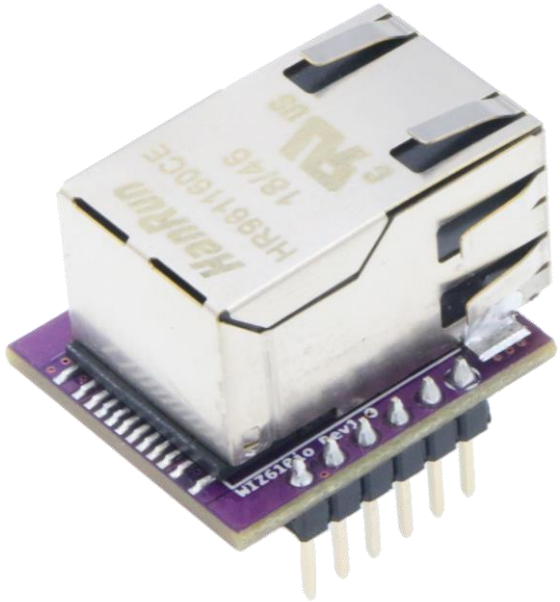
WIZ610io User Manual

(Version 1.0)



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Document Revision History

Date	Revision	Changes
2019-02-18	V1.0	Official Release

1. Introduction

WIZ610io is the internet offload network module that includes W6100 (TCP/IP hardwired chip, include PHY), MAG-JACK (RJ45 with X'FMR) with other glue logics. It can be used as a component and no effort is required to interface W6100 and Transformer.

The WIZ610io is an ideal option for users who want to develop their Internet enabling systems rapidly.

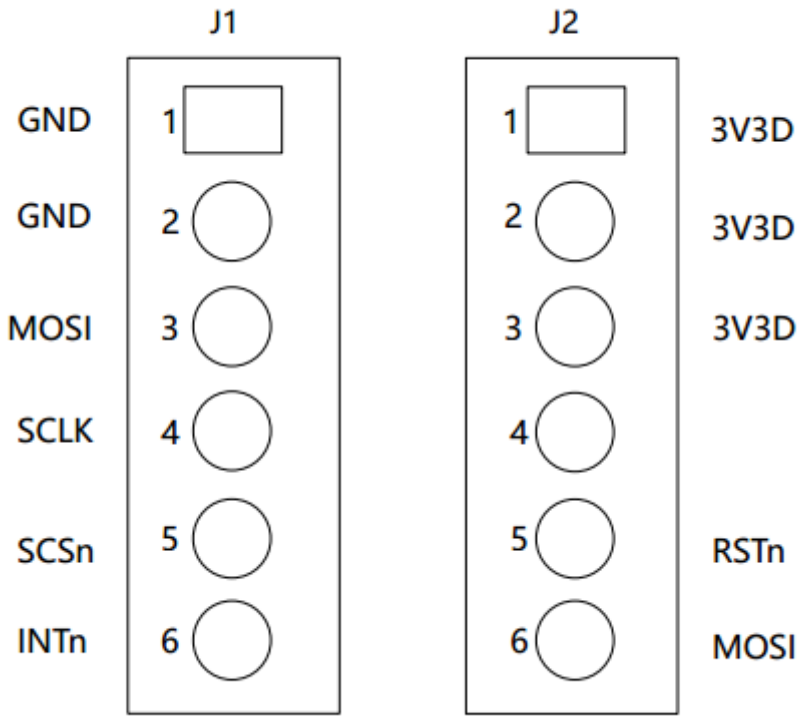
For the detailed information on implementation of Hardware TCP/IP, refer to the W6100 Datasheet.

WIZ610io consists of W6100 and MAG-JACK.

- TCP/IP, Ethernet MAC : W6100
- Ethernet PHY : Included in W6100
- Connector : MAG-JACK(RJ45 with Transformer)

1.1 Feature

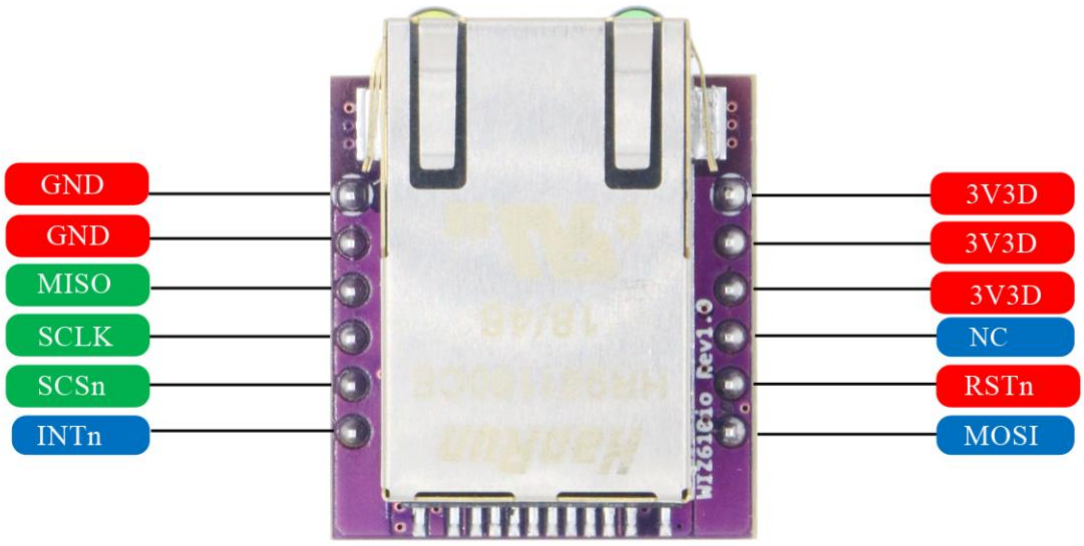
- Support Hardwired TCP/IP Protocols : TCP, UDP, IPv6, IPv4, ICMPv6, ICMPv4, IGMP, MLDv1, ARP, PPPoE
- Support IPv4/IPv6 Dual Stack
- Support 8 independent SOCKETs simultaneously with 32KB Memory
- Support SOCKET-less Command:
  ARP, PING, ICMPv6(PING, ARP,DAD,NA,RS) Command for IPv6 Auto-configuration& Network Monitoring
- Support Ethernet Power Down Mode & Main Clock Switching for power save
- Support Wake on LAN over UDP
- Support Serial Interface: High Speed SPI(MODE 0/3)
- Internal 16Kbytes Memory for TX/ RX Buffers
- 10BaseT/100BaseTX Ethernet PHY Integrated
- Support Auto Negotiation (Full and half duplex, 10 and 100-based)
- Support Auto-MDIX only on Auto-Negotiation Mode
- 3V operation with 5V I/O signal tolerance
- Network Indicator LEDs (Full/Half Duplex, Link, 10/100 Speed, Active)
- Interfaces with two 2.54mm pitch 1 x 10 header pin
- Temperature : -40 ~ 85℃(Operating)



2. Pin assignment & description

Type	Description
I	Input
O	Output
P	Power & Ground

2.1 Pin assignment



< TOP side view >

2.2 Pin description

Pin No.		I/O	Pin Name	Description
J1	1	P	GND	**Ground**
	2	P	GND	**Ground**
	3	I	MOSI	**SPI Master Out Slave In** This pin is used to SPI MOSI signal pin.
	4	I	SCLK	**SPI Clock** This pin is used to SPI Clock Signal pin.
	5	I	nSCS	**SPI Slave Select :** Active Low This pin is used to SPI Slave Select signal Pin when using SPI interface.
	6	O	INTn	**Interrupt** : Active low This pin indicates that W6100 requires MCU attention after socket connecting, disconnecting, data receiving timeout, and WOL (Wake on LAN). The interrupt is cleared by writing IR Register or Sn_IR (Socket n-th Interrupt Register). All interrupts are maskable.
J2	1	P	GND	**Ground**
	2	P	3V3D	**Power** : 3.3 V power supply
	3	P	3V3D	**Power** : 3.3 V power supply
	4	I	-	-
	5	I	RSTn	**Reset :** RSTn initializes W6100. RSTn must be asserted to Low longer than 500ns. After asserted RSTn, W6100 spends 60.3ms for initialization. Low : W6100 initialized. High : Normal Operation.
	6	O	MISO	**SPI Master In Slave Out** This pin is used to SPI MISO signal pin.

3. Device SPI operations

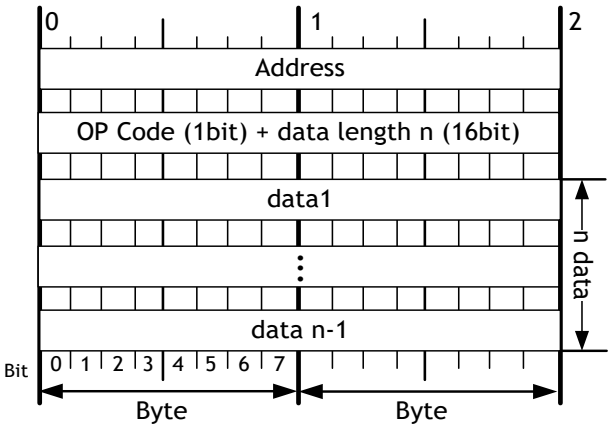
WIZ610io is controlled by a set of instruction that is sent from a external host , commonly referred to as the SPI Master. The SPI Master communicates with W6100 via the SPI bus, which is composed of four signal lines: Slave Chip Select (nSCS), Serial Clock (SCLK), MOSI (Master Out Slave In) and MISO (Master In Slave Out).

The SPI protocol defines four modes for its operation (Mode 0-3). Each mode differs according to the SCLK polarity and phase - how the polarity and phase control the flow of data on the SPI bus. The W6100 operates as SPI Slave device and supports the most common modes - SPI Mode 0 and 3.

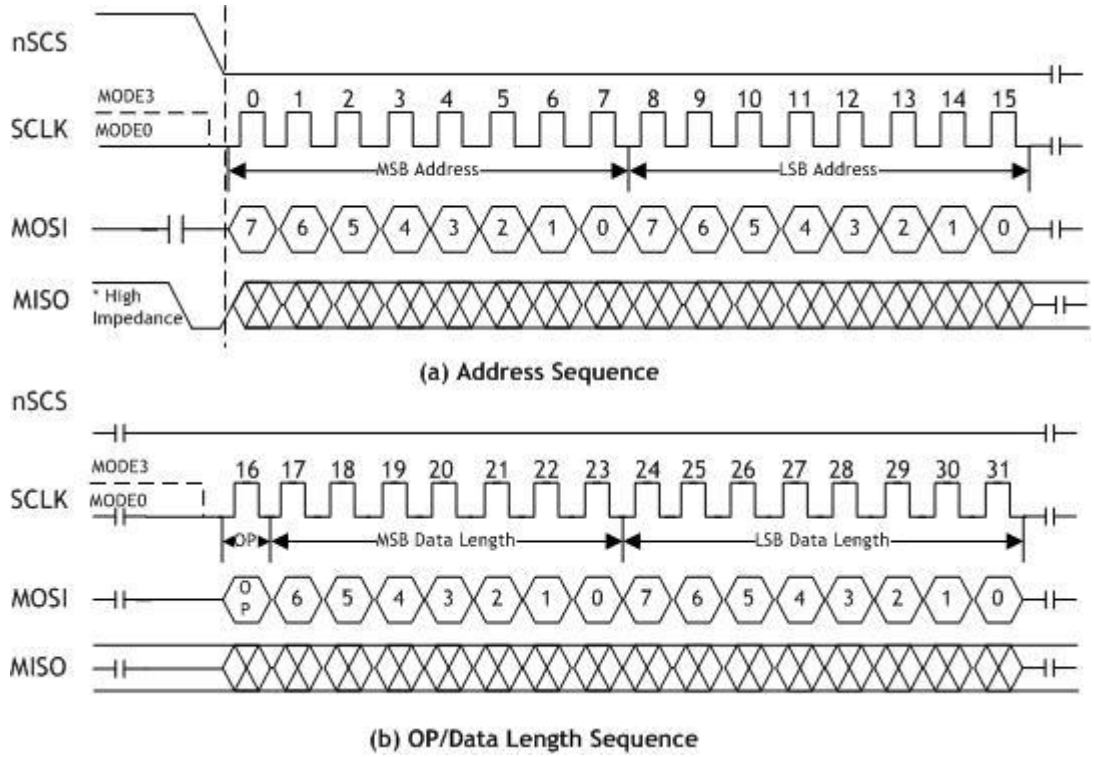
The only difference between SPI Mode 0 and 3 is the polarity of the SCLK signal at the inactive state. With SPI Mode 0 and 3, data is always latched in on the rising edge of SCLK and always output on the falling edge of SCLK.

3.1 Process of using general SPI Master device

1. Configure Input/Output direction on SPI Master Device pins.
2. Configure nSCS as 'High' on inactive
3. Write target address for transmission on SPDR register (SPI Data Register).
4. Write OP code and data length for transmission on SPDR register.
5. Write desired data for transmission on SPDR register.
6. Configure nSCS as 'Low' (data transfer start)
7. Wait for reception complete
8. If all data transmission ends, configure nSCS as 'High'



< W6100 SPI Frame Format >

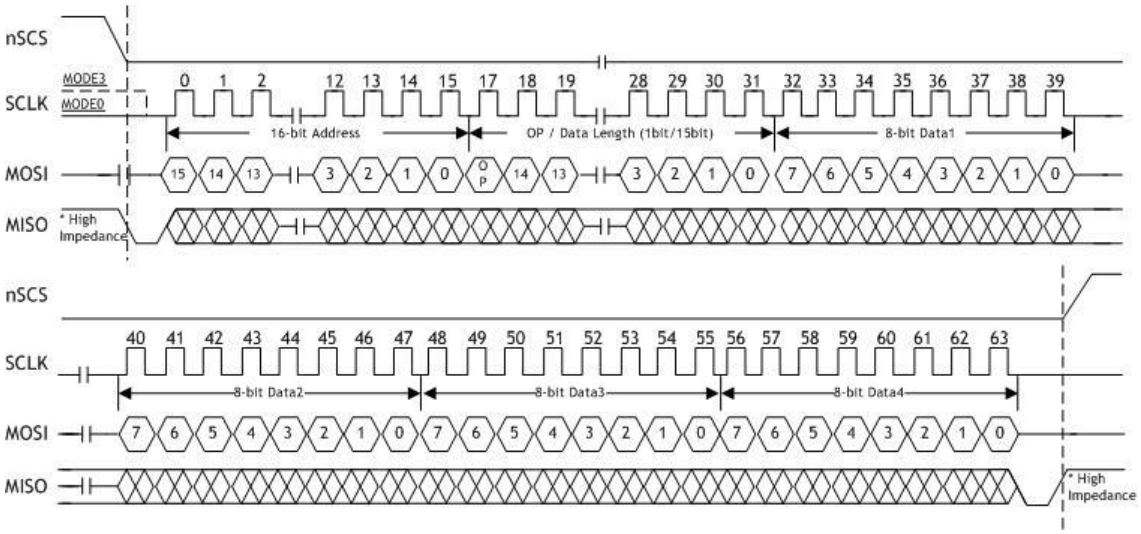


< Address and OP/DATA Length Sequence Diagram >

3.2 Read processing

The READ processing is entered by driving nSCS low, followed by the Address, the OP code, the Data Length and the Data byte on MOSI. The OP code (OP) is defined type of the READ OP and WIRTE OP. On OP = 0, the read operation is selected. Otherwise, On OP = 1, the write operation is selected.

In W6100 SPI mode, the Byte READ processing and the burst READ processing are provided. The Byte READ processing takes 4 instructions which is consist of the 16-bit Address, the 1-bit OP code(0x0), the 15-bit Data length and 8-bit Data. Otherwise, The Burst READ processing only takes the Data instruction after the setting of the burst read processing. To distinguish between the Byte READ and the burst READ processing, the Data length is used. If the Data length is '1,' the Byte READ processing is operated. Otherwise, the Burst READ Processing is operated when the Data length is more than two. The MISO pin should be selected by driving MISO low after the falling edge of the nSCS.



< Read Sequence >

```
/* Pseudo Code for Read data of 8bit per packet */
#define data_read_command      0x00
uint16 addr;        // Address : 16bits
int16 data_len;     // Data length :15bits
uint8 data_buf[];   // Array for data
SpiSendData();     // Send data from MCU to W6100
SpiRecvData();     // Receive data from   W6100 to MCU

{
ISR_DISABLE();   // Interrupt Service Routine disable
CSoff();   // CS=0, SPI start

// SpiSendData
SpiSendData(((addr+idx) & 0xFF00) >> 8);     // Address byte 1
SpiSendData((addr+idx) & 0x00FF);       // Address byte 2

// Data write command + Data length upper 7bits
SpiSendData((data_read_command| ((data_len& 0x7F00) >> 8)));
// Data length bottom 8bits
SpiSendData((data_len& 0x00FF));

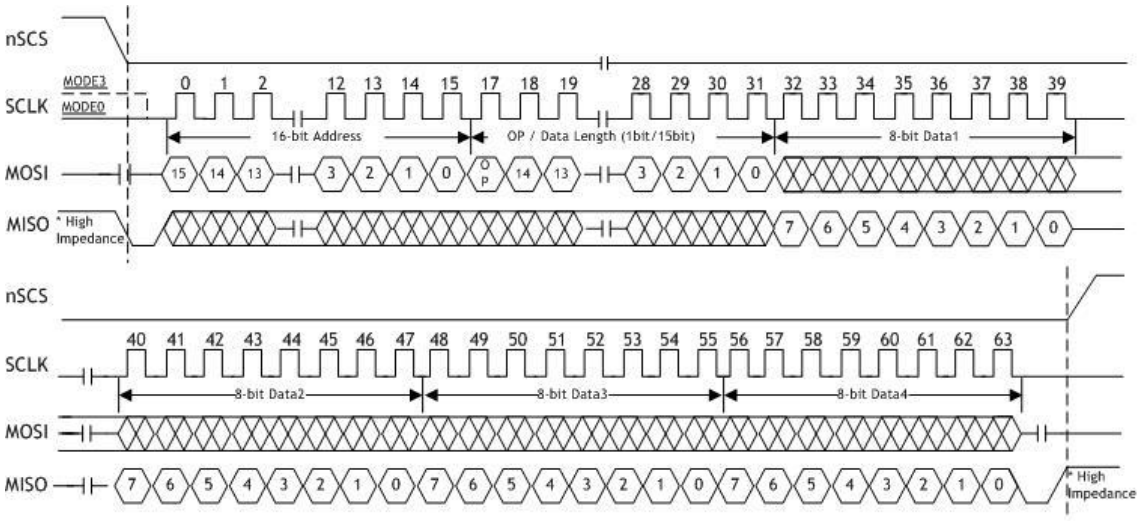
// Read data:On data_len> 1, Burst Read Processing Mode.
for(int idx = 0; idx<data_len; idx++)
{
```

```
    SpiSendData(0);    // Dummy data
    data_buf[idx] = SpiRecvData(idx);    // Read data
  }
  CSon();    // CS=1, SPI end
  ISR_ENABLE();    // Interrupt Service Routine disable
  }
```

3.3 Write processing

The WRITE processing is entered by driving nSCS low, followed by the Address, the OP code, the Data Length, and the Data byte on MISO.

In W6100 SPI mode, the Byte WRITE processing and the Burst WRITE processing are provided. The Byte WRITE processing takes 4 instructions which is consist of the 16-bit Address, the 1-bit OP code(0x1), the 15-bit Data length and 8-bit Data. Otherwise, The Burst WRITE processing only takes the Data instruction after the setting of the Burst WRITE processing. To distinguish between the Byte WRITE and the Burst WRITE processing, the Data length is used. If the Data length is '1,' the Byte WRITE processing is operated. Otherwise, the Burst WRITE Processing is operated when the Data length is more than two. The MOSI pin should be selected by driving MOSI low after the falling edge of the nSCS.



< Write Sequence >

```
/* Pseudo Code for Write data of 8bit per packet */
#define data_write_command      0x80
uint16 addr;       // Address : 16bits
int16 data_len;       // Data length :15bits
uint8 data_buf[];    // Array for data

{
SpiSendData();     //Send data from MCU to   W6100

ISR_DISABLE();// Interrupt Service Routine disable
CSoff();// CS=0, SPI start

SpiSendData(((addr+idx) & 0xFF00) >> 8);    // Address byte 1
SpiSendData((addr+idx) & 0x00FF);    // Address byte 2

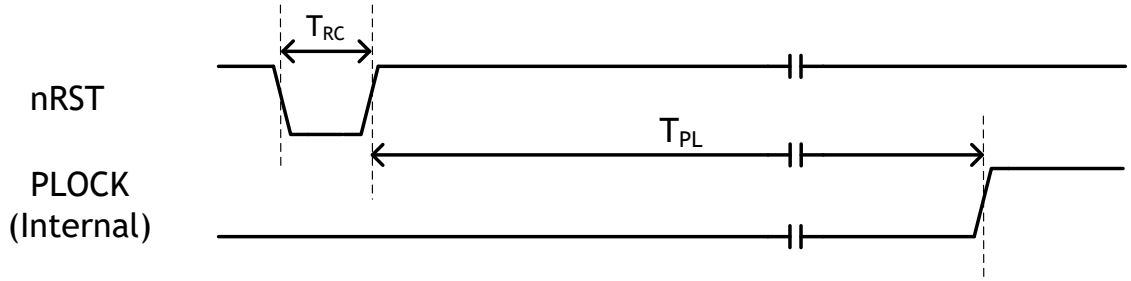
// Data write command + Data length upper 7bits
SpiSendData((data_write_command | ((data_len& 0x7F00) >> 8)));
// Data length bottom 8bits
SpiSendData((data_len& 0x00FF));

// Write data: On data_len> 1, Burst Write Processing Mode.
for(int idx = 0; idx<data_len; idx++)
    SpiSendData(data_buf[idx]);

CSon();    // CS=1, SPI end
IINCHIP_ISR_ENABLE();    // Interrupt Service Routine disable
}
```

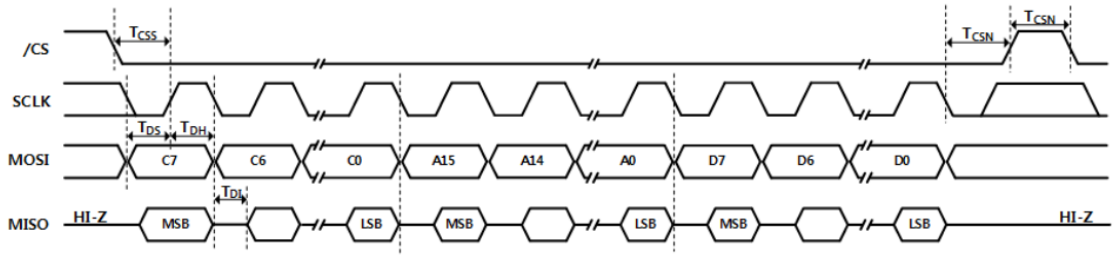
4. Timing diagram

4.1 Reset Timing



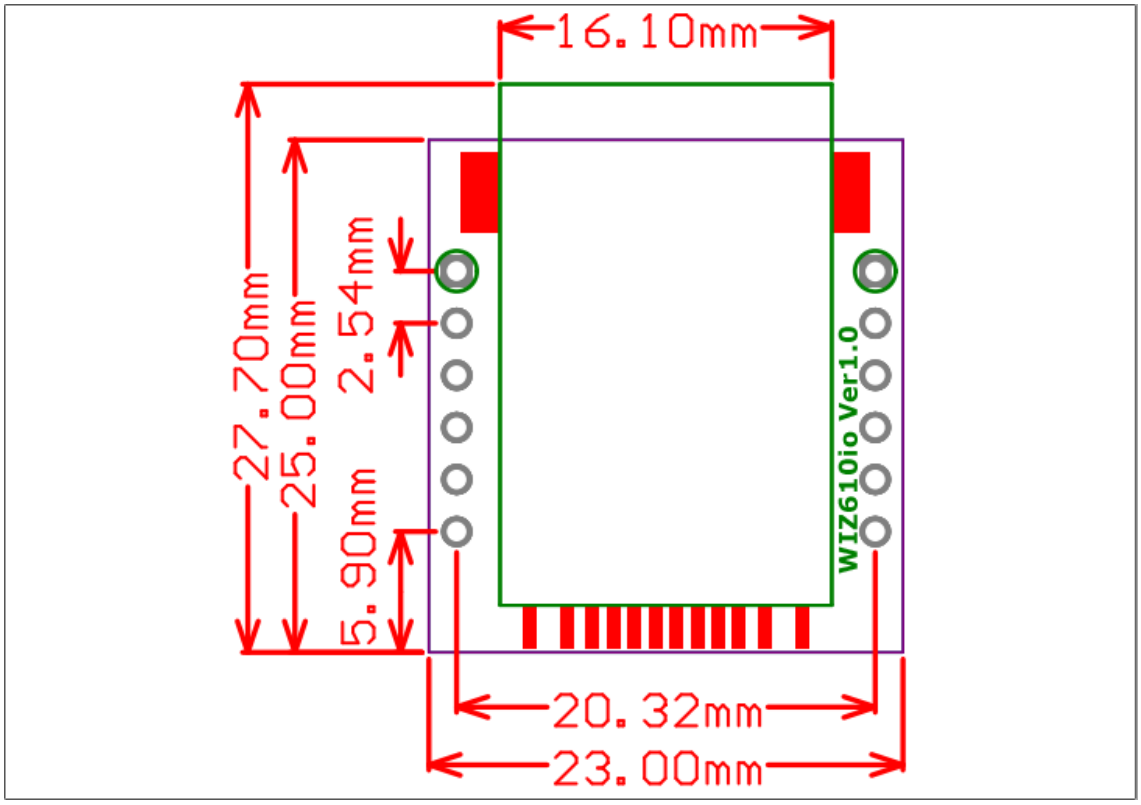
Symbol	Description	Min	Typ	Max
T_{RC}	Reset Cycle Time	210ns	330ns	560ns
T_{PL}	nRST internal PLOCK	-		60.3ms

4.2 SPI Timing

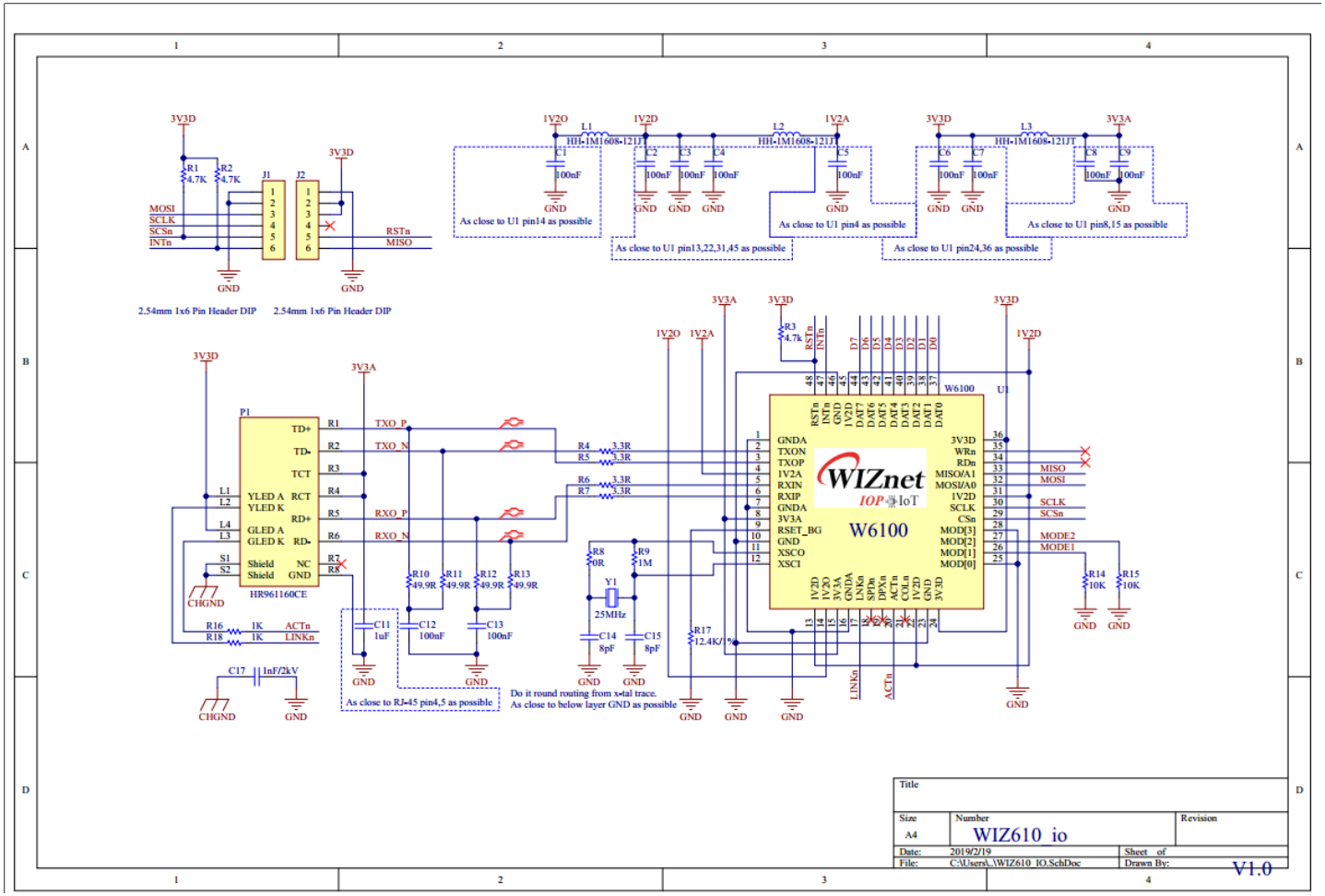


Symbol	Description	Min	Max	Units
F_{SCK}	SCK Clock Frequency		70	MHz
T_{CSS}	nSCS tup Time	3 SYS_CLK	-	ns
T_{CSN}	nSCS Next Time	2 SYS_CLK		ns
T_{DS}	Data In Setup Time	3		ns
T_{DH}	Data In Hold Time	3		ns
TDI	Data Invalid Time	7		ns
TDR	Data Ready Time	6 SYS_CLK + 30		ns

5. Dimensions



6. Reference Schematics



Comment	Description	Designator	Footprint	Quantity
100nF	Ceramic CAP 0603(1608)	C1, C2, C3, C4, C5, C6, C7, C8, C9, C12, C13	0603-C	11
1uF	Ceramic CAP 0603(1608)	C11	0603-C	1
8pF	Ceramic CAP 0603(1608)	C14, C15	0603-C	2
1nF/2kV	Ceramic CAP 1808(4520)	C17	CAP-1206	1
2.54mm 1x6 Pin Header DIP	2.54mm 1x6 Pin Header DIP	J1, J2	IDC-1X6	2
120R FB	Inductor 0603(1608)	L1, L2, L3	0603-L	3
HR961160CE		P1	RJ-45(HR961160CE)	1
4.7K	RES0603	R1, R2, R3	0603-R	3
3.3R	RES0603	R4, R5, R6, R7	0603-R	4
0R	RES0603	R8	0603-R	1
1M	RES0603	R9	0603-R	1
49.9R	RES0603	R10, R11, R12, R13	0603-R	4
10K	RES0603	R14, R15	0603-R	2
1K	RES0603	R16, R18	0603-R	2
12K/1%	RES0603	R17	RES-0603	1
300/1%	RES0603	R19	RES-0603	1
W6100	WIZnet Hardwired TCP/IP Chip	U1	WIZNET W6100 QFN	1
25MHz	X-tal 25MHz,3.2x2.5 SMD	Y1	OSC-82J0626	1

7. Warranty

WIZnet Co., Ltd. offers the following limited warranties applicable only to the original purchaser. This offer is non-transferable.

WIZnet warrants our products and its parts against defects in materials and workmanship under normal use for period of standard ONE(1) YEAR for the WIZ610io module and labor warranty after the date of original retail purchase. During this period, WIZnet will repair or replace a defective products or part free of charge.

Warranty Conditions:

1. The warranty applies only to products distributed by WIZnet or our official distributors.
2. The warranty applies only to defects in material or workmanship as mentioned above in 3.Warranty. The warranty applies only to defects which occur during normal use and does not extend to damage to products or parts which results from alternation, repair, modification, faulty installation or service by anyone other than someone authorized by WIZnet ; damage to products or parts caused by accident, abuse, or misuse, poor maintenance, mishandling, misapplication, or used in violation of instructions furnished by us ; damage occurring in shipment or any damage caused by an act of God, such as lightening or line surge.

Procedure for Obtaining Warranty Service

1. Contact an authorized distributors or dealer of WIZnet for obtaining an RMA (Return Merchandise Authorization) request form within the applicable warranty period.
2. Send the products to the distributors or dealers together with the completed RMA request form. All products returned for warranty must be carefully repackaged in the original packing materials.
3. Any service issue, please contact to sales@wiznet.io