STM809, STM810
STM811, STM812

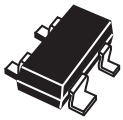
Reset circuit

Features

- Precision monitoring of 3 V, 3.3 V, and 5 V supply voltages
- Two output configurations
  - Push-pull $\overline{RST}$ output (STM809/811)
  - Push-pull RST output (STM810/812)
- 140 ms reset pulse width (min)
- Low supply current - 6 µA (typ)
- Guaranteed $\overline{RST}$/RST assertion down to V_{CC} = 1.0 V
- Operating temperature: –40 °C to 85 °C (industrial grade)
- Lead-free, small SOT23 and SOT143 package



SOT23-3 (WX)



SOT143-4 (W1)

Table 1. Device summary

	Active-low reset	Active-high reset	Manual reset input	Package
STM809	✔			SOT23-3
STM810		✔		SOT23-3
STM811	✔		✔	SOT143-4
STM812		✔	✔	SOT143-4

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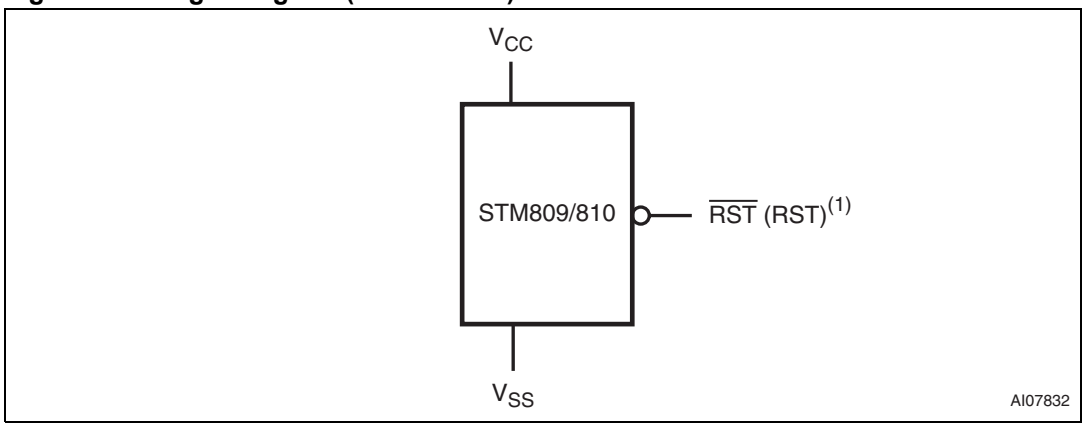
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1 Description

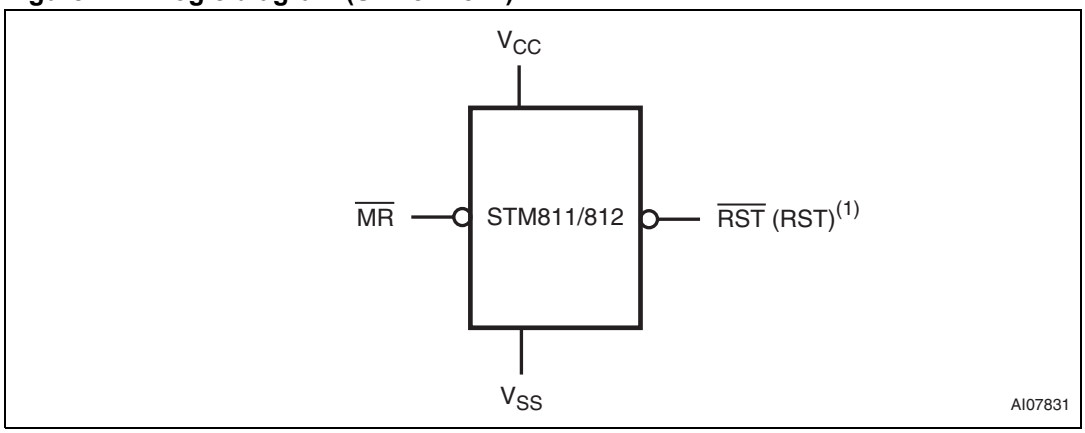
The STM809/810/811/812 microprocessor reset circuits are low-power supervisory devices used to monitor power supplies. They perform a single function: asserting a reset signal whenever the V_{CC} supply voltage drops below a preset value and keeping it asserted until V_{CC} has risen above the preset threshold for a minimum period of time (t_{rec}). The STM811/812 also provide a push-button reset input ($\overline{MR}$).

Figure 1. Logic diagram (STM809/810)



1. For STM810

Figure 2. Logic diagram (STM811/812)



1. For STM812

Table 2. Signal names

V_{SS}	Ground
$\overline{RST}$	Active-low reset output
RST(1)	Active-high reset output
V_{CC}	Supply voltage
$\overline{MR}$(2)	Manual reset input

1. STM810/812 only
2. STM811/812 only

Figure 3. SOT23-3 connections

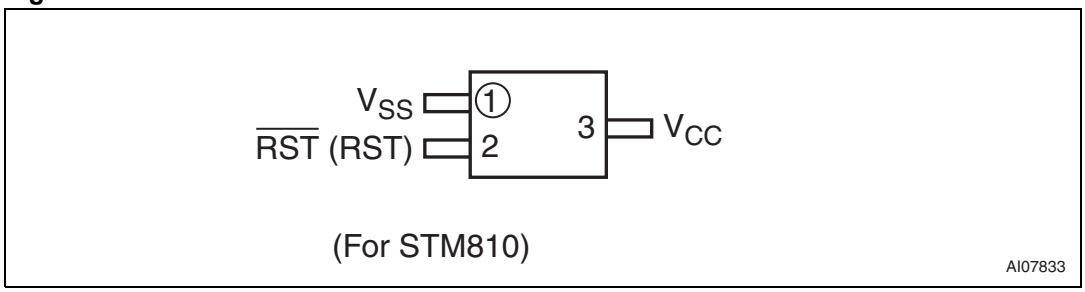


Figure 4. SOT143-4 connections

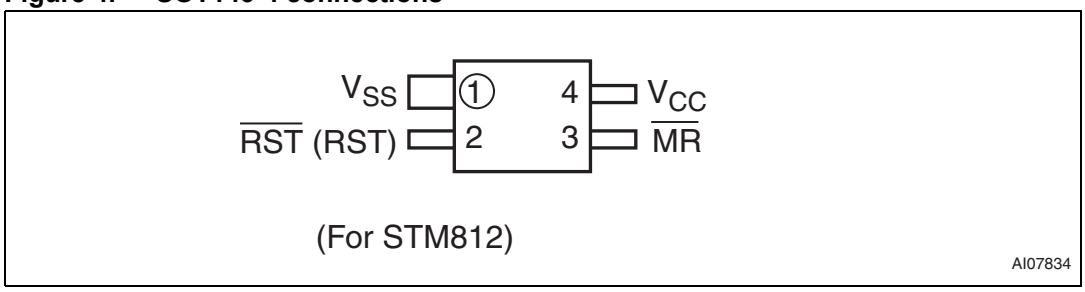
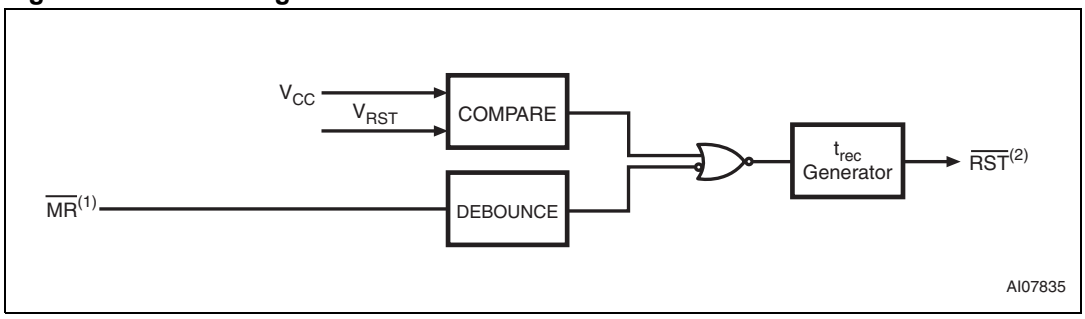
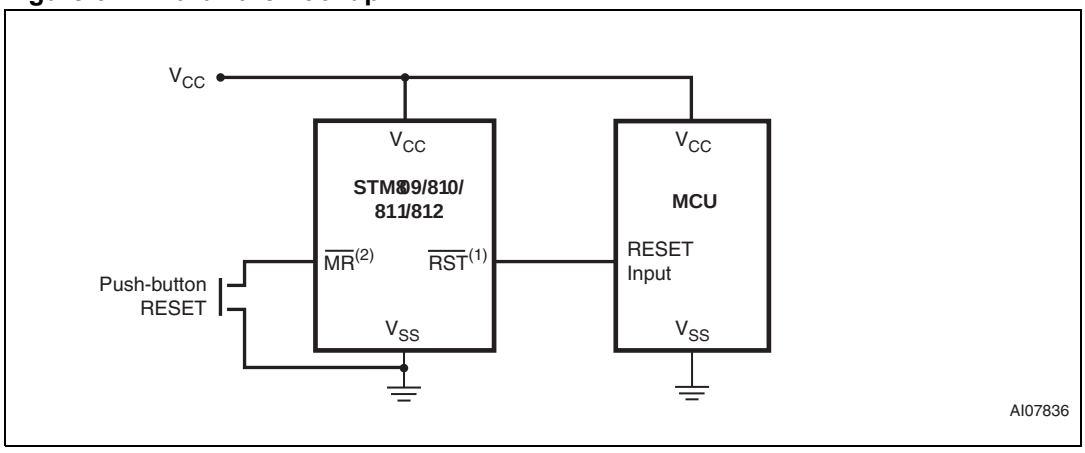


Figure 5. Block diagram



1. STM811/812 only
2. RST for STM810/812

Figure 6. Hardware hookup



1. STM809/811 only (RST for STM810/812)
2. STM811/812 only

2 Operation

2.1 Reset output

The STM809/810/811/812 microprocessor reset circuit asserts a reset signal to the MCU whenever V_{CC} goes below the reset threshold (V_{RST}), or when the push-button reset input ($\overline{MR}$) is taken low (see *Figure 14 on page 13*). $\overline{RST}$ (active high for STM810/812) is guaranteed valid down to V_{CC} = 1 V (0° to 70°C).

During power-up, once V_{CC} exceeds the reset threshold an internal timer keeps $\overline{RST}$ low for the reset time-out period, t_{rec}. After this interval, $\overline{RST}$ returns high.

If V_{CC} drops below the reset threshold, $\overline{RST}$ goes low. Each time $\overline{RST}$ is asserted, it stays low for at least the reset time-out period. Any time V_{CC} goes below the reset threshold, the internal timer clears. The reset timer starts when V_{CC} returns above the reset threshold. The active-low reset ($\overline{RST}$) and active-high reset (RST) both source and sink current.

2.2 Push-button reset input (STM811/812)

A logic low on $\overline{MR}$ asserts $\overline{RST}$. $\overline{RST}$ remains asserted while $\overline{MR}$ is low, and for t_{rec} after it returns high. The $\overline{MR}$ input has an internal 20 kΩ pull-up resistor, allowing it to be left open if not used. This input can be driven with TTL/CMOS-logic levels or with open-drain/collector outputs. Connect a normally open push-button switch from $\overline{MR}$ to GND to create a manual reset function; external debounce circuitry is not required. If the device is used in a noisy environment, connect a 0.1 µF capacitor from $\overline{MR}$ to GND to provide additional noise immunity.

2.3 Negative-going V_{CC} transients

The STM809/810/811/812 are relatively immune to negative-going V_{CC} transients (glitches). *Figure 12 on page 11* shows typical transient duration versus reset comparator overdrive (for which the STM809/810/811/812 will NOT generate a reset pulse). The graph was generated using a negative pulse applied to V_{CC}, starting at 0.5V above the actual reset threshold and ending below it by the magnitude indicated (comparator overdrive). The graph indicates the maximum pulse width a negative V_{CC} transient can have without causing a reset pulse. As the magnitude of the transient increases (further below the threshold), the maximum allowable pulse width decreases. Any combination of duration and overdrive which lies under the curve will NOT generate a reset signal. Typically, a V_{CC} transient that goes 100 mV below the reset threshold and lasts 20 µs or less will not cause a reset pulse. A 0.1 µF bypass capacitor mounted as close as possible to the V_{CC} pin provides additional transient immunity.

2.4 Valid $\overline{\text{RST}}$ output down to V_{CC} = 0 V

When V_{CC} falls below 1 V, the $\overline{\text{RST}}$ (STM809/811) output no longer sinks current, but becomes an open circuit. In most systems this is not a problem, as most MCUs do not operate below 1 V. However, in applications where $\overline{\text{RST}}$ output must be valid down to 0 V, a pull-down resistor may be added to hold the $\overline{\text{RST}}$ output low. This resistor must be large enough to not load the $\overline{\text{RST}}$ output, and still be small enough to pull the output to ground. A 100 kΩ resistor is recommended.

Note: The same situation applies for the active-high RST of the STM810/812. A 100 kΩ pull-up resistor to V_{CC} should be used if RST must remain valid for V_{CC} < 1.0 V.

3 Typical operating characteristics

Note: Typical values are at T_A = 25 °C, V_{CC} = 5 V for L/M versions, V_{CC} = 3.3 V for T/S versions, and V_{CC} = 3.0 V for R versions.

Figure 7. Supply current vs. temperature, L/M/R/S/T (no load)

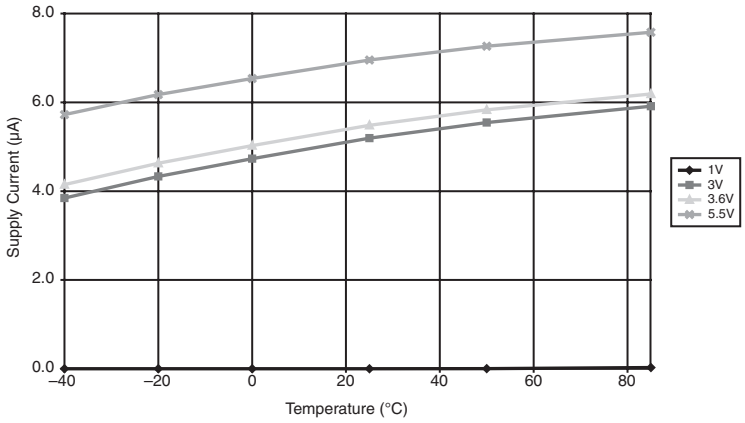


Figure 8. Power-down reset delay vs. temperature - $V_{OD} = V_{TH} – V_{CC}$ (L/M)

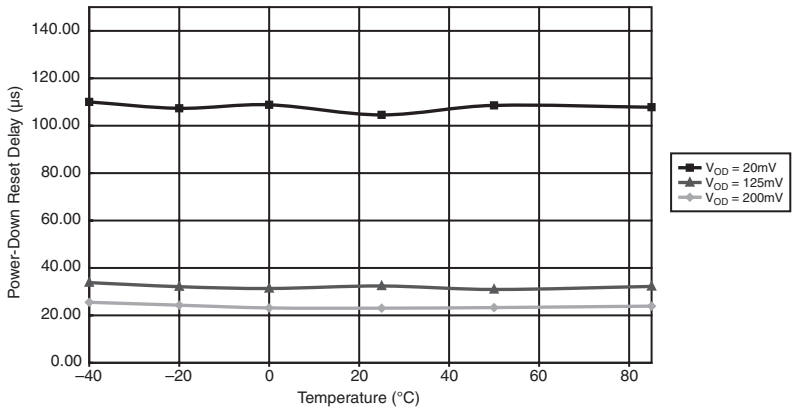


Figure 9. Power-down reset delay vs. temperature - $V_{OD} = V_{TH} – V_{CC}$ (R/S/T)

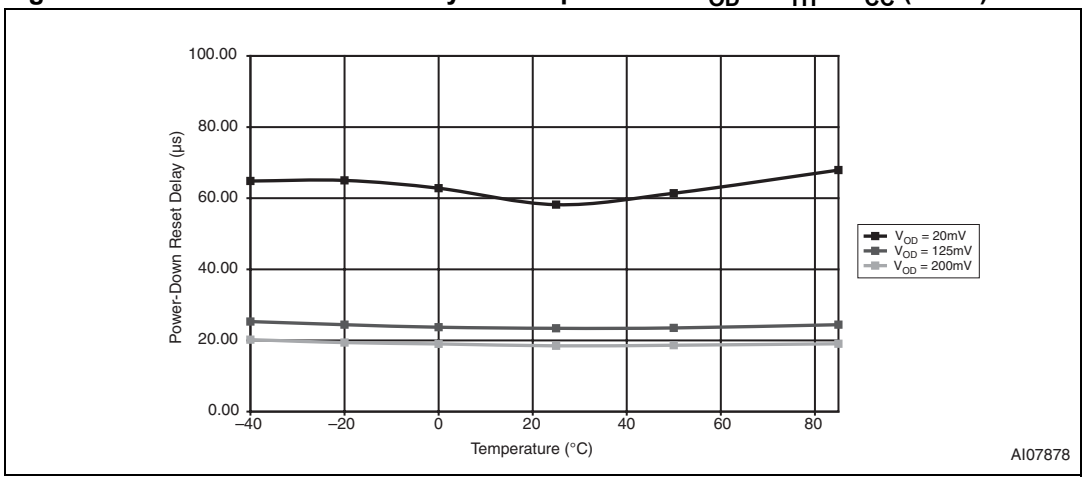


Figure 10. Power-up t_{rec} vs. temperature

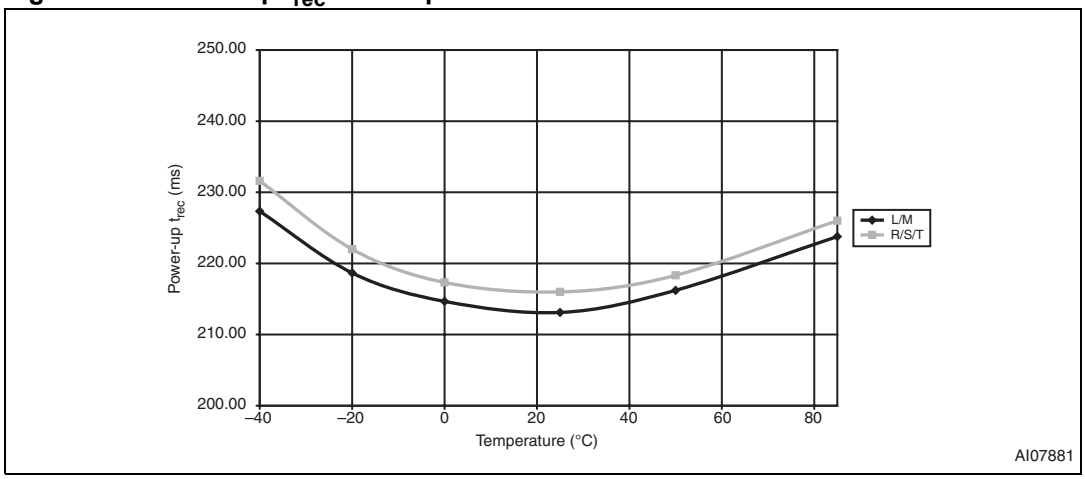


Figure 11. Normalized reset threshold vs. temperature

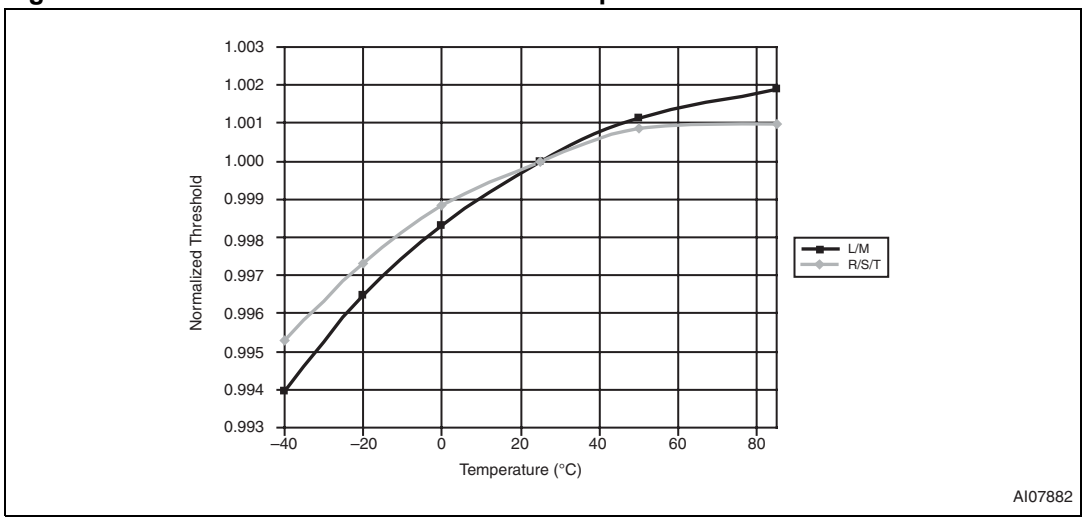
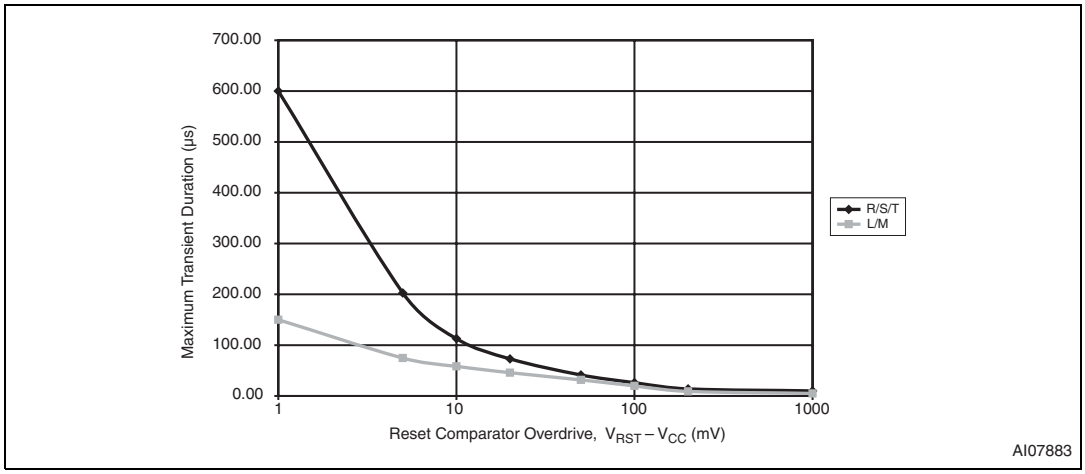


Figure 12. Max transient duration NOT causing reset pulse vs. reset comparator overdrive



4 Maximum ratings

Stressing the device above the rating listed in the absolute maximum ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
T_{STG}	Storage temperature (V_{CC} off)	–55 to 150	°C
T_{SLD}(1)	Lead solder temperature for 10 seconds	260	°C
V_{IO}	Input or output voltage	–0.3 to V_{CC} +0.3	V
V_{CC}	Supply voltage	–0.3 to 7.0	V
I_O	Output current	20	mA
P_D	Power dissipation	320	mW

1. Reflow at peak temperature of 260 °C. The time above 255 °C must not exceed 30 seconds.

5 DC and AC parameters

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics tables that follow, are derived from tests performed under the measurement conditions summarized in *Table 4.*. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

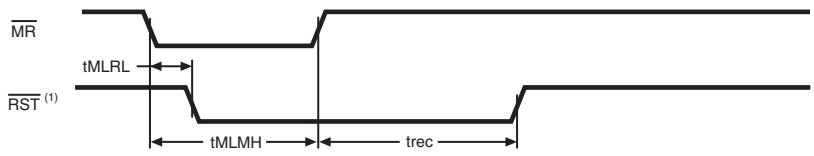
Table 4. Operating and AC measurement conditions

Parameter	STM809/810/811/812	Unit
V_{CC} supply voltage	1.0 to 5.5	V
Ambient operating temperature (T_A)	–40 to 85	°C
Input rise and fall times	≤ 5	ns
Input pulse voltages	0.2 to 0.8 V_{CC}	V
Input and output timing ref. voltages	0.3 to 0.7 V_{CC}	V

Figure 13. AC testing input/output waveforms



Figure 14. $\overline{MR}$ timing waveform



1. RST for STM810/812

Table 5. DC and AC characteristics

Sym	Alter-native	Description	Test condition(1)		Min	Typ	Max	Unit
V_{CC}		Operating voltage	T_A = –40 to +85 °C		1.2		5.5	V
			T_A = 0 to +70 °C		1.0		5.5	V
I_{CC}		V_{CC} supply current	V_{CC} < 3.6 V			5.5	10	µA
			V_{CC} < 5.5 V			7	15	µA
V_{IH}		$\overline{MR}$ input high voltage	V_{CC} > V_{RST} (max), STM8XXL/M		2.2			V
			V_{CC} > V_{RST} (max), STM8XXR/S/T		0.7 V_{CC}			V
V_{IL}		$\overline{MR}$ input low voltage	V_{CC} > V_{RST} (max), STM8XXL/M				0.8	V
			V_{CC} > V_{RST} (max), STM8XXR/S/T				0.25 V_{CC}	V
V_{OL}		$\overline{RST}$ output low voltage (active high(2) or low)	STM8XXR/S/T only, I_{OL} = 1.2 mA V_{CC} = V_{RST} (min)				0.3	V
			STM8XXL/M only, I_{OL} = 3.2 mA V_{CC} = V_{RST} (min)				0.4	V
V_{OL}		$\overline{RST}$ output low voltage	I_{OL} = 50 µA; V_{CC} > 1.0 V				0.3	V
V_{OH}		$\overline{RST}$ output high voltage	STM8XXR/S/T only, I_{OH} = 500 µA		0.8 V_{CC}			V
			STM8XXL/M only, I_{OH} = 800 µA		0.8 V_{CC}			V
		RST output high voltage	I_{OH} = 150 µA, 1.8 V < V_{CC} < V_{RST} (min)		0.8 V_{CC}			V
Reset thresholds								
V_{RST}		Reset threshold	STM8XXL	25 °C	4.56	4.63	4.70	V
				–40 to 85 °C	4.50		4.75	V
			STM8XXM	25 °C	4.31	4.38	4.45	V
				–40 to 85 °C	4.25		4.50	V
			STM8XXT	25 °C	3.04	3.08	3.11	V
				–40 to 85 °C	3.00		3.15	V
			STM8XXS	25 °C	2.89	2.93	2.96	V
				–40 to 85 °C	2.85		3.00	V
			STM8XXR	25 °C	2.59	2.63	2.66	V
				–40 to 85 °C	2.55		2.70	V
		V_{RST} temperature coefficient	V_{CC} = 3.3 V			45		ppm/ °C
		V_{CC} to $\overline{RST}$ delay	V_{CC} = V_{RST} to (V_{RST} – 100 mV)	STM8XXL/M		40		µs
				STM8XXR/S/T		20		µs

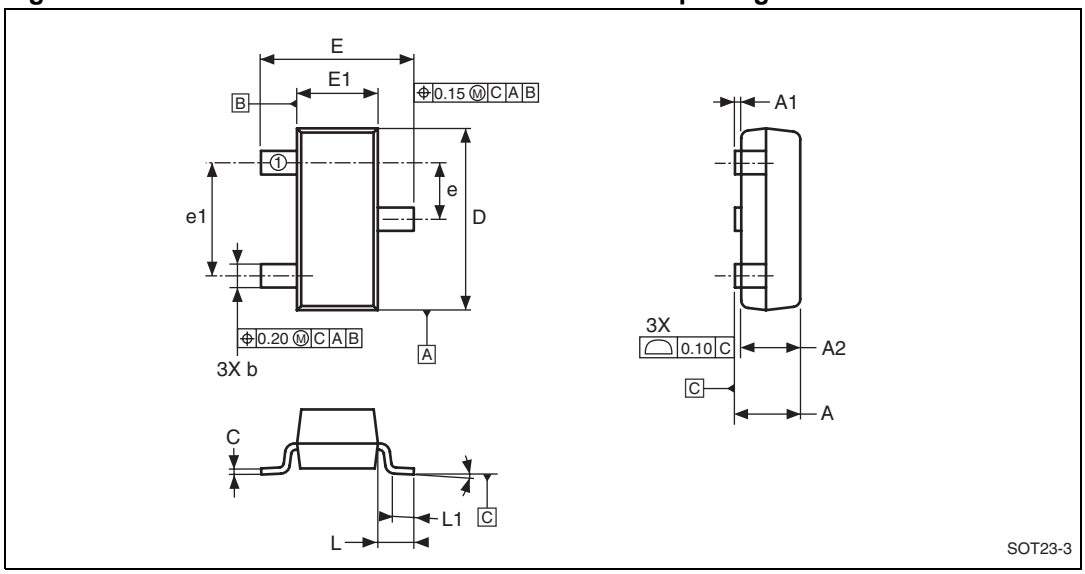
Sym	Alter-native	Description	Test condition(1)	Min	Typ	Max	Unit
Push-button reset input							
$t_{\overline{MLMH}}$	$t_{\overline{MR}}$	$\overline{MR}$ pulse width		10			µs
$t_{\overline{MLRL}}$	$t_{\overline{MRD}}$	$\overline{MR}$ to $\overline{RST}$ output delay(3)			0.5		µs
		$\overline{MR}$ glitch immunity(4)			100		ns
		$\overline{MR}$ pull-up resistance		10	20	30	kΩ
	t_{rec}	$\overline{RST}$ pulse width		140	210	280	ms

1. Valid for ambient operating temperature: T_A = –40 to 85 °C; V_{CC} = 1.2 V to 5.5 V (except where noted).
2. For active high (RST); $V_{CC} = V_{RST}$ (max)
3. RST output for STM810/812
4. “Glitches” of 100 ns or less typically will not generate a reset pulse.

6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 15. SOT23-3 – 3-lead small outline transistor package outline

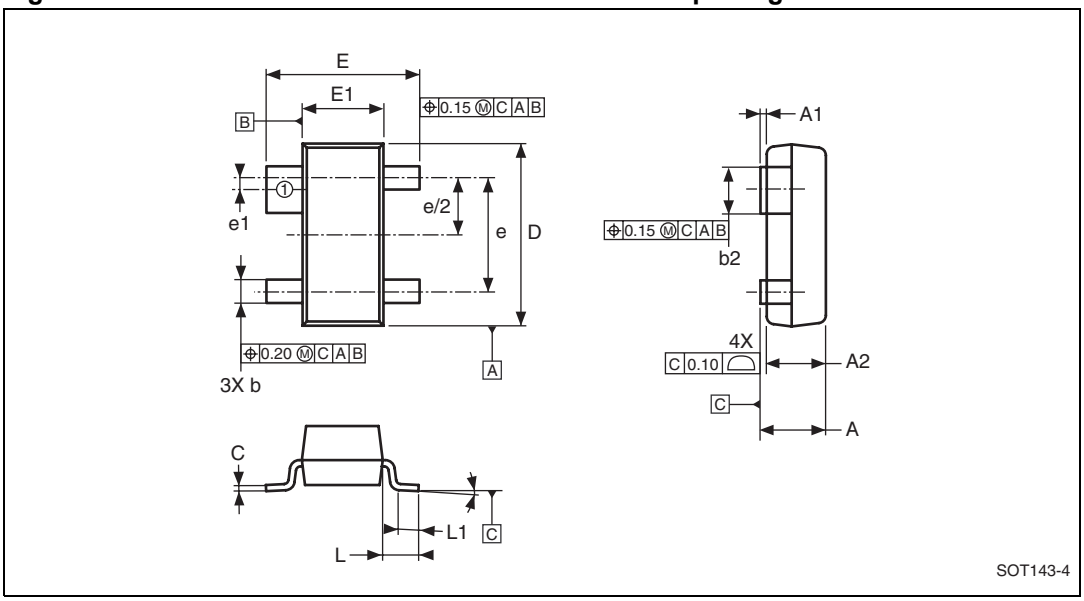


Note: Drawing is not to scale.

Table 6. SOT23-3 – 3-lead small outline transistor package mechanical data

Symbol	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		0.89	1.12		0.035	0.044
A1		0.01	0.10		0.001	0.004
A2		0.88	1.02		0.035	0.042
b		0.30	0.50		0.012	0.020
C		0.08	0.20		0.003	0.008
D		2.80	3.04		0.110	0.120
E		2.10	2.64		0.083	0.104
E1		1.20	1.40		0.047	0.055
e		0.89	1.03		0.035	0.041
e1		1.78	2.05		0.070	0.081
L	0.54			0.021		
L1		0.40	0.60		0.016	0.024
Θ		0°	8°		0°	8°
N	3			3		

Figure 16. SOT143-4 – 4-lead small outline transistor package outline



Note: Drawing is not to scale.

Table 7. SOT143-4 – 4-lead small outline transistor package mechanical data

Symbol	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		0.89	1.12		0.035	0.044
A1		0.01	0.10		0.001	0.004
A2		0.88	1.02		0.035	0.042
b		0.37	0.51		0.015	0.020
b2		0.76	0.94		0.030	0.037
C		0.09	0.18		0.004	0.007
D		2.80	3.04		0.110	0.120
E		2.10	2.64		0.083	0.104
E1		1.20	1.40		0.047	0.055
e	1.92			0.076		
e1	0.20			0.008		
L	0.55			0.022		
L1		0.40	0.60		0.016	0.024
Θ		0°	10°		0°	10°
N	4			4		

7 Part numbering

Table 8. Ordering information scheme

Example: STM8XX L WX 6 F

Device type

STM8XX

Reset threshold voltage

L = V_{RST} = 4.50 V to 4.75 V

M = V_{RST} = 4.25 V to 4.50 V

T = V_{RST} = 3.00 V to 3.15 V

S = V_{RST} = 2.85 V to 3.00 V

R = V_{RST} = 2.55 V to 2.70 V

Package

WX = SOT23-3 (STM809, STM810)

W1 = SOT143-4 (STM811, STM812)

Temperature range

6 = –40 to 85 °C

Shipping method

F = ECOPACK® package, tape & reel

For a list of available options (e.g., speed, package) or for further information on any aspect of this device, please contact the ST sales office nearest to you.

Table 9. Marking description

Part number	Reset threshold	Output	Topside marking(1)
STM809L	4.63 V	Push-pull $\overline{RST}$	8AAx
STM809M	4.38 V	Push-pull $\overline{RST}$	8ABx
STM809T	3.08 V	Push-pull $\overline{RST}$	8ACx
STM809S	2.93 V	Push-pull $\overline{RST}$	8ADx
STM809R	2.63 V	Push-pull $\overline{RST}$	8AEx
STM810L	4.63 V	Push-pull RST	8AFx
STM810M	4.38 V	Push-pull RST	8AGx
STM810T	3.08 V	Push-pull RST	8AHx
STM810S	2.93 V	Push-pull RST	8AJx
STM810R	2.63 V	Push-pull RST	8AKx
STM811L	4.63 V	Push-pull $\overline{RST}$	8ALx
STM811M	4.38 V	Push-pull $\overline{RST}$	8AMx
STM811T	3.08 V	Push-pull $\overline{RST}$	8ANx
STM811S	2.93 V	Push-pull $\overline{RST}$	8APx
STM811R	2.63 V	Push-pull $\overline{RST}$	8AQx
STM812L	4.63 V	Push-pull RST	8ARx
STM812M	4.38 V	Push-pull RST	8ASx
STM812T	3.08 V	Push-pull RST	8ATx
STM812S	2.93 V	Push-pull RST	8AUx
STM812R	2.63 V	Push-pull RST	8AVx

1. x = letter assigned to indicate assembly work week (i.e., A = WW01 and WW02, B = WW03 and WW04, C = WW05 and WW06..., Z = WW51, WW52, and WW53).

8 Revision history

Table 10. Document revision history

Date	Revision	Changes
02-Sep-2003	1	First issue
03-Oct-2003	1.1	Update operating characteristics (*Figure 7*, *Figure 8*, *Figure 9*, *Figure 10*, *Figure 11*, *Figure 12*)
16-Oct-2003	1.2	Update characteristics (*Table 5*); modify illustration (*Figure 12*)
17-Nov-2003	1.3	Modified with JEDEC timing symbols (*Figure 14*;*Table 5*)
04-Dec-2003	2	Reformatted; promoted; updated (*Figure 14*; *Table 5*, *6*)
09-Dec-2003	2.1	Correct timing label, combine characteristics (*Figure 10*; *Table 5*)
10-Feb-2004	3	Clarify package; update DC characteristics (*Table 5*, *Table 8*)
19-Nov-2004	4	Update dimensions (*Table 6*).
05-Jan-2010	5	Updated footnote in *Table 3*, added text to *Section 6: Package mechanical data*, added footnote to *Table 9*.

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