LR645

High-Input Voltage SMPS, Start-up/Linear Regulator

Features

- Accepts inputs from 15 to 450V
- Output currents: up to 3.0mA continuous, 30mA peak
- Supply current typically 50µA
- Line regulation typically 0.1mV/V
- Output can be trimmed from 8.0 to 12V
- Output current can be increased to 150mA with external FET

Applications

- Off-line SMPS startup circuits (pulse loads)
- Low power off-line regulators
- Regulators for noisy inputs

Description

LR645 is a high-input voltage, low-output current, linear regulator that is available in two versions. A 3-terminal, fixed-output voltage version is available in TO-92, TO-220 and SOT-89 packages, as well as an adjustable voltage version available in an 8-lead SOIC package.

The 3-terminal version of LR645 functions like any other low-voltage, 3-terminal regulator except it allows the use of much higher-input voltages. When used in a Switched-mode Power Supply (SMPS), start-up circuit, LR645 eliminates the need for large power resistors. In this application, current is drawn from the high voltage line only during start-up. Only leakage current flows after start-up, thereby reducing the continuous power dissipation to a few milliwatts.

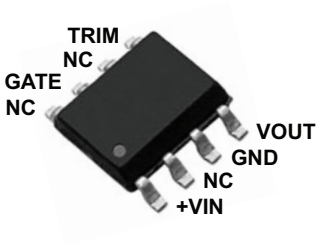
The adjustable-voltage version allows trimming of the output voltage from 8.0 to 12V. This version can also be connected to an external depletion mode metal–oxide–semiconductor field-effect transistor (MOSFET) for increased output current. When used in conjunction with depletion mode MOSFET DN2540N5, an output current of up to 150mA is achieved.

WARNING

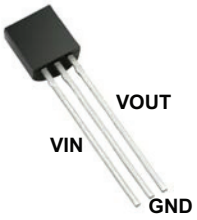
The LR645 does NOT provide galvanic isolation. When operated from an AC line, potentially lethal voltages can be present on the IC. Adequate means of protecting the end user from such voltages must be provided by the circuit developer.

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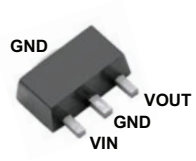
Package Type



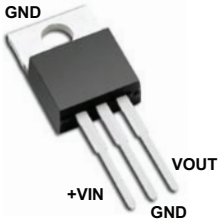
8-Lead SOIC



TO-92



TO-243AA (SOT-89)



TO-220

See Table 2-1 for pin information

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1.0 ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Input Voltage 450V
Output voltage 15.5V
Operating and storage temperature ..... -55°C to +150°C

Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions, above those indicated in the operational listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

1.1 ELECTRICAL SPECIFICATIONS

TABLE 1-1: ELECTRICAL CHARACTERISTICS [1]

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{OUT}	Output voltage	9.3	10	10.7	V	No load
	Output voltage over temperature[2]	9.0	10	11.5	V	T_J = - 40 to +125°C, No load
ΔV_{OUT}	Line regulation	-	40	200	mV	V_{IN} = 15 to 400V, No load
	Load regulation	-	150	400	mV	V_{IN} = 50V, I_{OUT} = 0 to 3.0mA
V_{IN}	Operating input voltage range	15	-	450	V	
I_{INQ}	Input quiescent current	-	50	150	µA	No Load
I_{OFF}	VIN off-state leakage current	-	0.1	10	µA	$V_{AUX} \geq V_{OUT}$ +1V applied to V_{OUT} pin
I_{AUX}	Input current to V_{OUT}	-	-	200	µA	$V_{AUX} \geq V_{OUT}$ +1V applied to V_{OUT} pin
$\Delta V_{OUT}/\Delta V_{IN}$	Ripple rejection ratio[2]	50	60	-	dB	120 Hz, No Load
e_n	Noise voltage[2]	-	25	-	µV	0.01 to 100 KHz
I_{PEAK}	Output peak current[3]	-	30	-	mA	C_{OUT} = 10 µF, V_{IN} = 400V
V_{AUX}	External voltage applied to V_{OUT}	-	-	13.2	V	
8-lead, adjustable voltage version only						
V_{OUT}	Output regulation trim range[2]	8	-	12	V	No load
ΔV_{OUT}	Load regulation at 8V trim[2]	-	200	400	mV	V_{IN} = 15V, I_{OUT} = 0 to 1.0 mA
	Load regulation at 12V trim[2]	-	100	400	mV	V_{IN} = 50V, I_{OUT} = 0 to 3.0 mA

1 Test Conditions unless otherwise specified: T_A = 25°C, V_{IN} = 15V-450V, C_{OUT} = 0.01 µF
2 Guaranteed by design
3 Pulse test duration <1.0 msec, duty cycle <2%

TABLE 1-2: THERMAL CHARACTERISTICS[1]

Package	θja	Power Dissipation @T_A=25°C
8-lead SOIC	101°C/W	0.31
TO-92	132°C/W	0.74
TO-220	29°C/W	1.8
TO-243AA (SOT-89)	133°C/W	1.6

1 Mounted on FR5 board; 25mm x 25mm x 1.57mm. Significant P_D increase possible on ceramic substrate.

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2.0 PIN DESCRIPTION

The locations of the pins are listed in Package Type.

TABLE 2-1: PIN DESCRIPTION

Function	Description
VIN	Regulator input. 8 - 450V.
GND	Ground return for all internal circuitry. This pin must be electrically connected to circuit common.
GATE	Output GATE driver for an external N-channel depletion.
TRIM	A voltage divider from V_{OUT} to this pin adjusts the output voltage.
VOUT	Regulator output.
NC	No connection.

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3.0 FUNCTIONAL DESCRIPTION

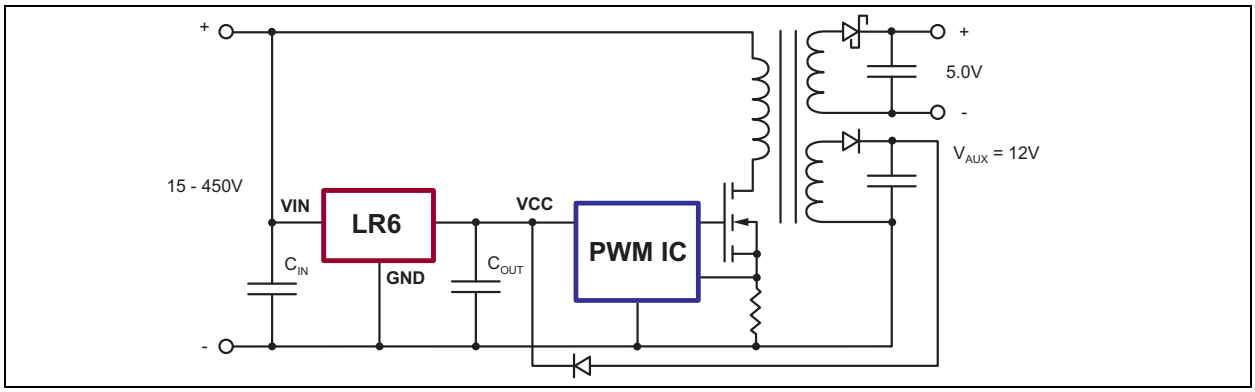
3.1 SMPS Start-Up Circuit

One of the main applications for LR645 is a start-up circuit for off-line, switch-mode power supplies (SMPS), as shown in Figure 3-1. A minimum output capacitance of 10 nF is recommended for stability. The wide operating, input voltage range of LR645 allows the SMPS to operate and start-up from rectified AC, or a DC voltage of 15 to 450V, without adjustment.

During start-up, the LR645 powers the V_{CC} line of the Pulse-Width Modulation (PWM) IC with a nominal output voltage of 10V. The auxiliary voltage connected through a diode to the V_{OUT} pin of LR645 will start to increase. When the auxiliary voltage becomes larger than the output voltage LR645 turns OFF both its internal high voltage input line and output voltage, allowing the auxiliary voltage to power the V_{CC} line of the PWM IC. After startup, LR645 doesn't draw any input current from the high-voltage line other than the leakage current of the internal MOSFET switch, which is typically 0.1µA.

The 3-terminal version shown in Figure 3-1 has load regulation guaranteed from 0 to 3.0mA at a fixed nominal output voltage of 10V. Applications requiring higher output current and/or a different output voltage can use the 8 pin adjustable version.

FIGURE 3-1: SMPS START-UP CIRCUIT

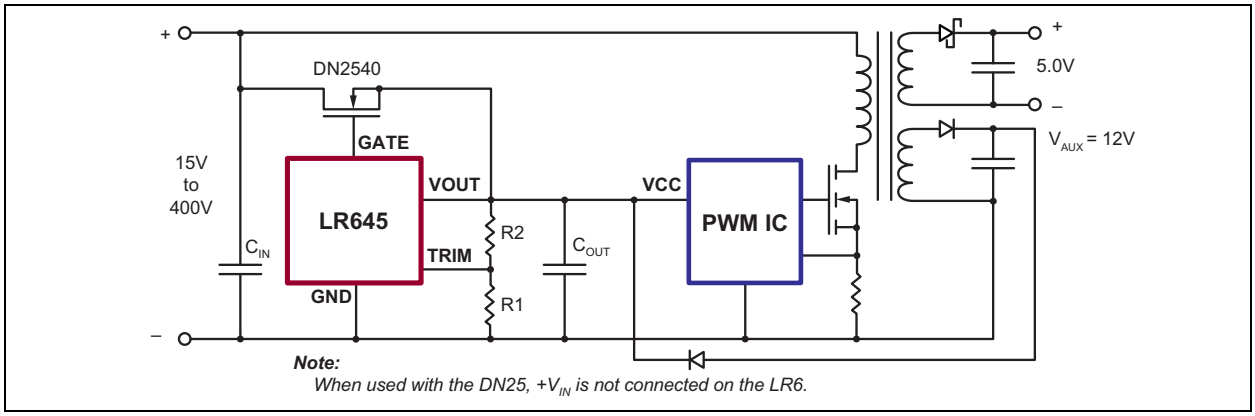


3.2 High-Current SMPS Start-Up Circuit

The 8-lead version of LR645 has connections for an external depletion-mode MOSFET for higher-output current and external resistors for adjustable-output voltage. As shown in Figure 3-2, the output current is increased to 150mA by using the DN2540, a 400V depletion-mode MOSFET. The maximum operating input voltage will be limited by the drain-to-source, breakdown voltage of the external MOSFET, but cannot exceed the 450V rating of LR645.

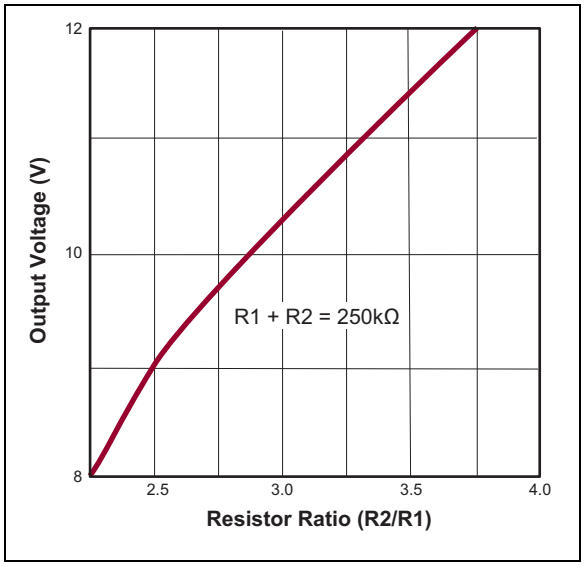
The output voltage can be adjusted from 8 to 12V with two external resistors: R1 and R2. The ratio of R2/R1 determines the output voltage. R2 is connected between the V_{OUT} and TRIM pins; R1 is connected between TRIM and GND pins. Figure 3-3 is a curve showing output voltage versus resistor ratio R2/R1. The optimum range for R1 + R2 is 200KΩ to 300KΩ. This minimizes loading and optimizes accuracy of the output voltage. Figure 3-3 uses an R1 + R2 of 250KΩ.

FIGURE 3-2: HIGH-CURRENT SMPS START-UP CIRCUIT



Note: *When used with the DN25, $+V_{IN}$ is not connected on the LR6.*

FIGURE 3-3: TYPICAL OUTPUT VOLTAGE VS RESISTOR RATIO



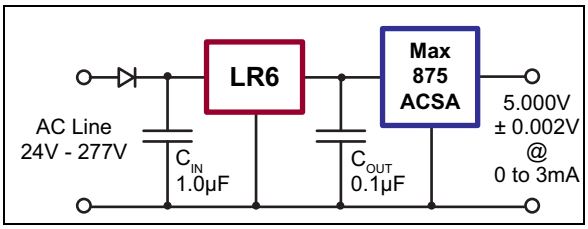
3.3 Off Line Linear Regulator

Circuits that require low voltages to operate logic and analog circuits benefit from LR645. The conventional use of step-down transformers can be eliminated, thereby saving space and cost. Some examples of low-voltage applications are: proximity controlled light switches, street lamp controls, and low-voltage power supplies for appliances such as washing machines, dishwashers, and refrigerators.

The wide operating-input voltage range of 15 to 450V, as well as the ripple rejection ratio of 50dB minimum, allows the use of a small, high-voltage input capacitor. The input AC line can be either full-wave or half-wave rectified. A minimum output capacitance of 0.01µF is recommended for output stability.

Figure 3-4 shows the LR645 as a pre-regulator to a precision regulator for high precision regulation. Higher output current is also possible by using an external depletion-mode MOSFET DN2540N5 as shown in Figure 3-5.

FIGURE 3-4: CASCADING FOR PRECISION



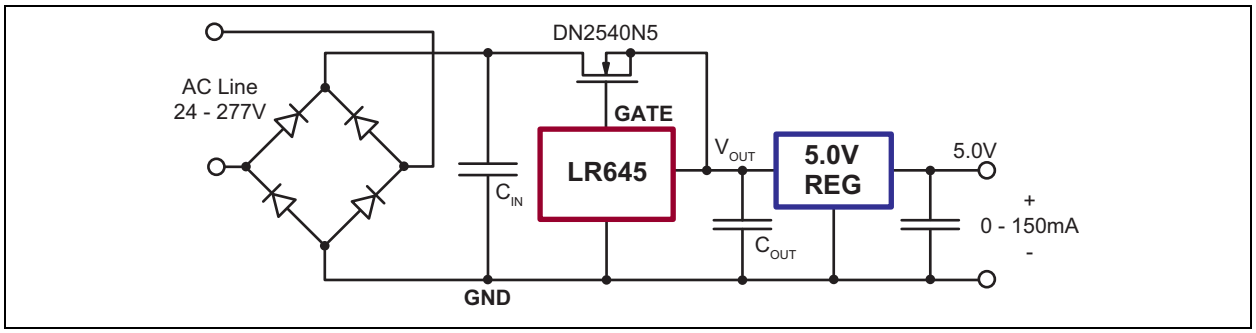
3.4 Power Dissipation Considerations

LR645 is a true linear regulator. Its power dissipation is therefore a function of input voltage and output load current. For example, if the LR645 provides a continuous load current of 3mA at 10V, while its input voltage is 400V, total dissipation in the LR645 will be:

$$P_{DISS} = (V_{IN} - V_{OUT}) \times (I_{OUT} + I_{MAXQuiescent})$$
$$= (400V - 10V) \times (3.0mA + 150\mu A)$$
$$= 1.23Watts$$

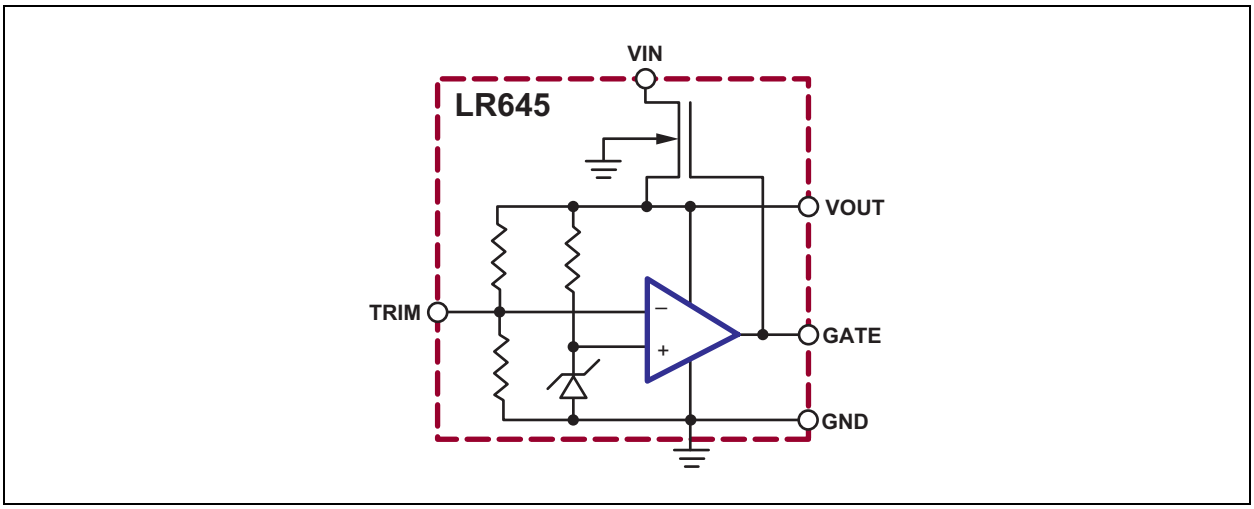
The 1.23 watts is for continuous operation. This is within the dissipation capabilities of the TO-220 and SOT-89 packages. See Table 1-2 on Page 3 for deratings. For SMPS start-up applications, the output current is usually required only during start-up. This duration depends upon the auxiliary supply output capacitor and C_{OUT}, but is typically a few hundred milliseconds. All package types of the LR645 have been characterized for use with a C_{OUT} of at least 10µF, and an AC line of 277V.

FIGURE 3-5: HIGH-CURRENT REGULATION



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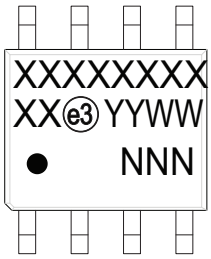
FIGURE 3-6: BLOCK DIAGRAM



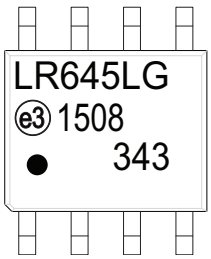
4.0 PACKAGING INFORMATION

4.1 Package Marking Information

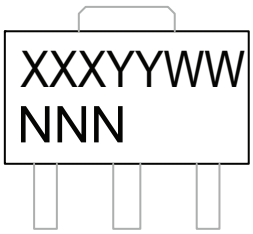
8-lead SOIC



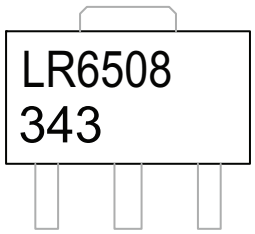
Example



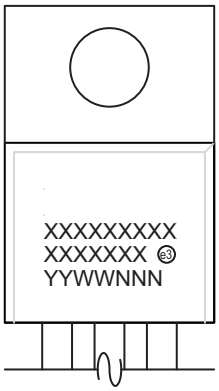
3-lead TO-243AA * (SOT-89)



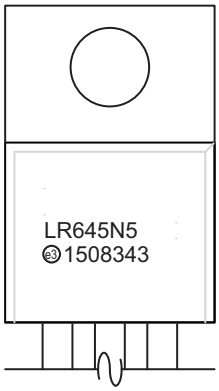
Example



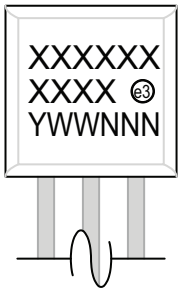
3-lead TO-220



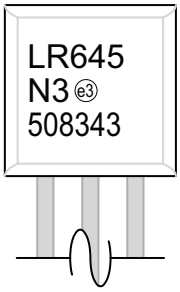
Example



3-lead TO-92



Example



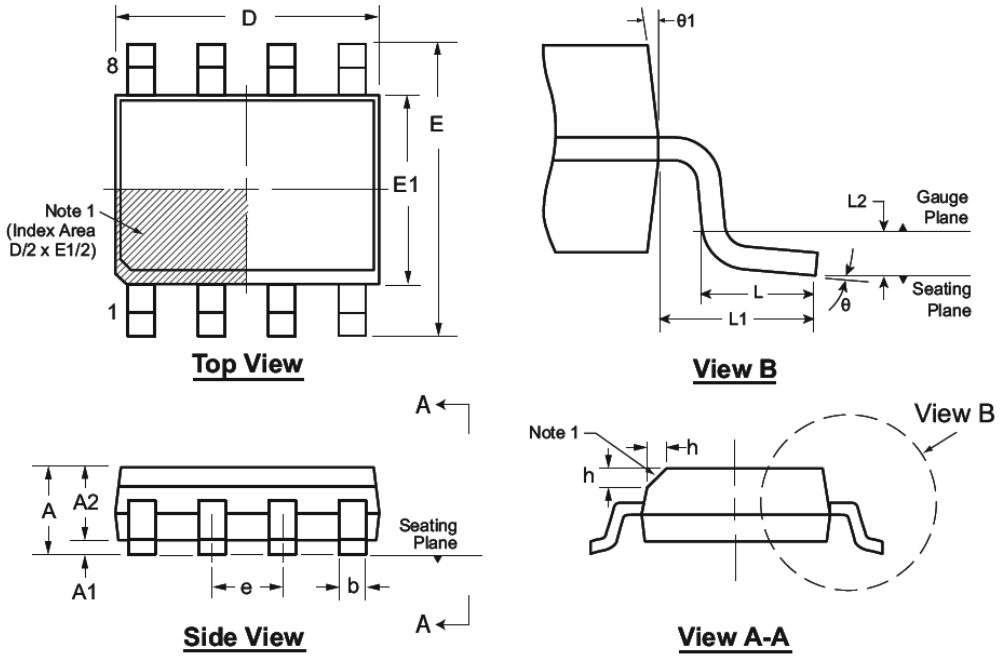
Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

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8-Lead SOIC (Narrow Body) Package Outline (LG/TG)

4.90x3.90mm body, 1.75mm height (max), 1.27mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Note:

1. *This chamfer feature is optional. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

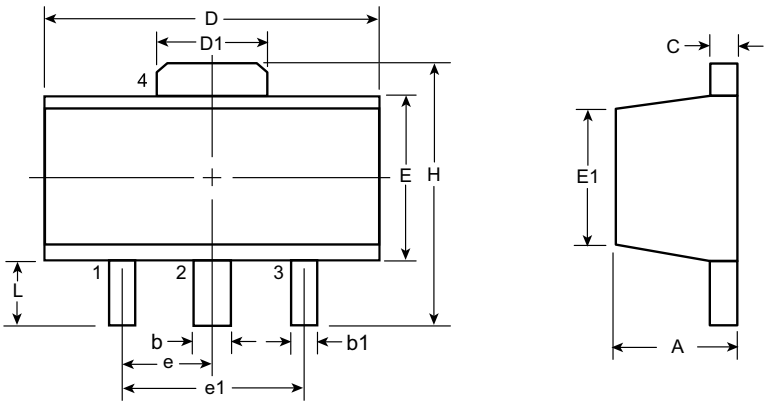
Symbol		A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	1.35*	0.10	1.25	0.31	4.80*	5.80*	3.80*	1.27 BSC	0.25	0.40	1.04 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	4.90	6.00	3.90		-	-			-	-
	MAX	1.75	0.25	1.65*	0.51	5.00*	6.20*	4.00*		0.50	1.27			8°	15°

JEDEC Registration MS-012, Variation AA, Issue E, Sept. 2005.

**** This dimension is not specified in the JEDEC drawing.***

Drawings are not to scale.

3-Lead TO-243AA (SOT-89) Package Outline (N8)



Top View **Side View**

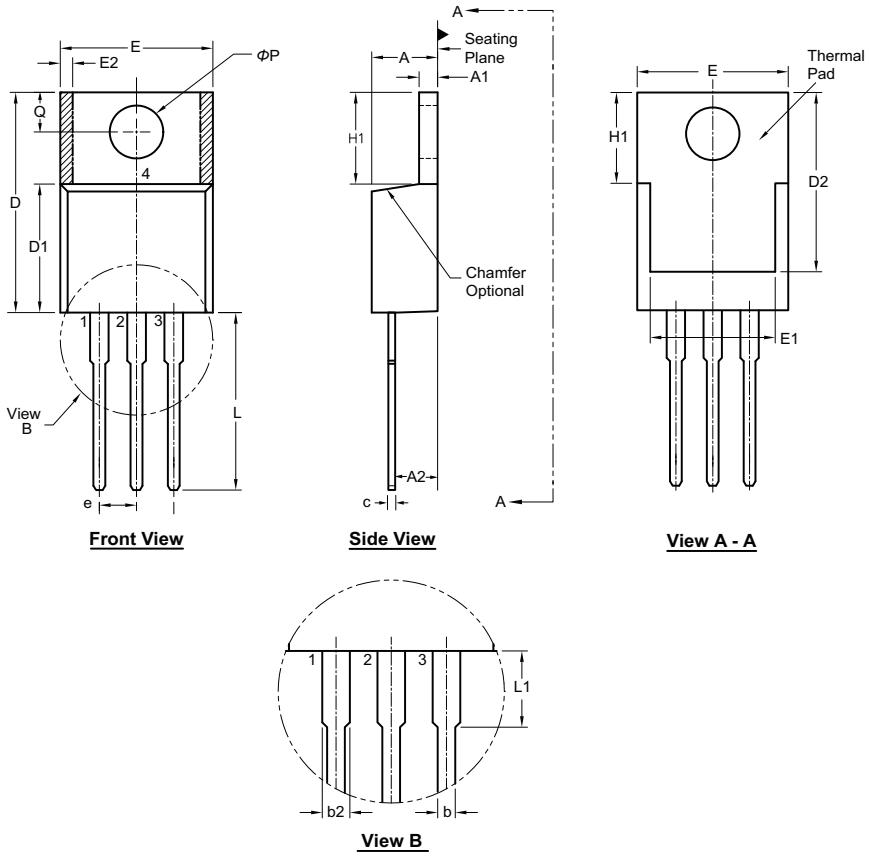
Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Symbol		A	b	b1	C	D	D1	E	E1	e	e1	H	L
Dimensions (mm)	MIN	1.40	0.44	0.36	0.35	4.40	1.62	2.29	2.00†	1.50 BSC	3.00 BSC	3.94	0.73†
	NOM	-	-	-	-	-	-	-	-			-	-
	MAX	1.60	0.56	0.48	0.44	4.60	1.83	2.60	2.29			4.25	1.20

JEDEC Registration TO-243, Variation AA, Issue C, July 1986.
† This dimension differs from the JEDEC drawing
Drawings not to scale.

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3-Lead TO-220 Package Outline (N5)

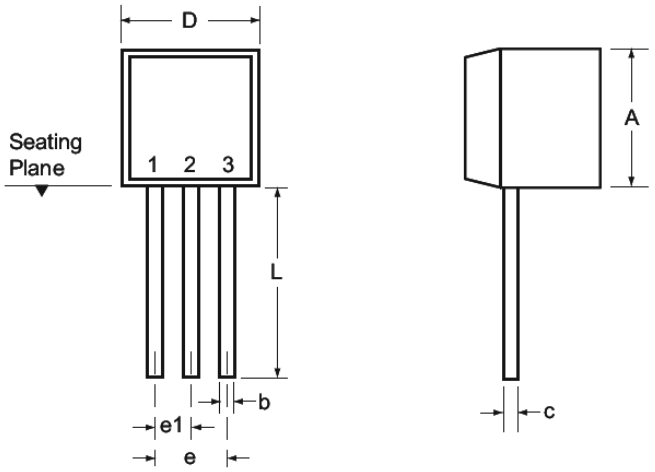


Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

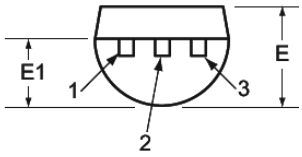
Symbol		A	A1	A2	b	b2	c	D	D1	D2	E	E1	E2	e	H1	L	L1	Q	ΦP
Dimension (inches)	MIN	.140	.020	.080	.015	.045	.012†	.560	.326†	.474†	.380	.270	0.20*	.100 BSC	.230	.500	.200*	.100	.139
	NOM	-	-	-	.027	.057	-	-	-	-	-	-	-		-	-	-	-	-
	MAX	.190	.055	.120†	.040	.070	.024	.650	.361†	.507	.420	.350	.030		.270	.580	.250	.135	.161

JEDEC Registration TO-220, Variation AB, Issue K, April 2002.
** This dimension is not specified in the JEDEC drawing.*
† This dimension differs from the JEDEC drawing.
Drawings not to scale.

3-Lead TO-92 Package Outline (L/LL/N3)



Front View **Side View**



Bottom View

Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Symbol		A	b	c	D	E	E1	e	e1	L
Dimensions (inches)	MIN	.170	.014†	.014†	.175	.125	.080	.095	.045	.500
	NOM	-	-	-	-	-	-	-	-	-
	MAX	.210	.022†	.022†	.205	.165	.105	.105	.055	.610*

JEDEC Registration TO-92.
** This dimension is not specified in the JEDEC drawing.*
† This dimension differs from the JEDEC drawing.
Drawings not to scale.

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APPENDIX A: REVISION HISTORY

Revision A (April 2015)

- Update file to new format

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	XX	-	X	-	X
Device	Package Options		Environmental		Media Type

Device:	LR645	= High-Input, Voltage SMPS, Start-up/Linear Regulator
Package:	LG	= 8-lead SOIC (adjustable voltage)
	N3	= TO-92 (fixed voltage)
	N5	= TO-220(fixed voltage)
	N8	= TO-243AA (SOT-89) (fixed voltage)
Environmental	G	= Lead (Pb)-free/ROHS-compliant package
Media Type:	(blank)	= 3300/Reel for LG packages = 1000/Bag for N3 packages = 50/Tube for TO-220 packages = 2000/Reel for TO-243AA packages
	P003	= 2000/Reel for N3 package
	P013	= 2000/Ammo Pack for N3 package

Examples:

a)	LR645LG-G:	8-lead SOIC package, 3300/reel.
b)	LR645N3-G	TO-92 package, 1000/bag
c)	LR645N3-G-P003:	TO-92 package, 2000/reel.
d)	LR645N3-G-P013:	TO-92 package, 2000/ammo pack.
e)	LR645N5-G	TO-220 package, 50/tube
f)	LR645N8-G	TO-243AA package, 2000/reel

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Note the following details of the code protection feature on Microchip devices:

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ISBN: 978-1-63277-244-2

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