LAN8710A/LAN8710Ai

Small Footprint MII/RMII 10/100 Ethernet Transceiver with HP Auto-MDIX and flexPWR® Technology

Highlights

- Single-Chip Ethernet Physical Layer Transceiver (PHY)
- Comprehensive flexPWR® Technology
  - Flexible Power Management Architecture
  - LVCMOS Variable I/O voltage range: +1.6V to +3.6V
  - Integrated 1.2V regulator with disable feature
- HP Auto-MDIX support
- Small footprint 32-pin QFN/SQFN lead-free RoHS compliant packages (5 x 5mm)

Target Applications

- Set-Top Boxes
- Networked Printers and Servers
- Test Instrumentation
- LAN on Motherboard
- Embedded Telecom Applications
- Video Record/Playback Systems
- Cable Modems/Routers
- DSL Modems/Routers
- Digital Video Recorders
- IP and Video Phones
- Wireless Access Points
- Digital Televisions
- Digital Media Adapters/Servers
- Gaming Consoles
- POE Applications (Refer to Application Note 17.18)

Key Benefits

- High-Performance 10/100 Ethernet Transceiver
  - Compliant with IEEE802.3/802.3u (Fast Ethernet)
  - Compliant with ISO 802-3/IEEE 802.3 (10BASE-T)
  - Loop-back modes
  - Auto-negotiation
  - Automatic polarity detection and correction
  - Link status change wake-up detection
  - Vendor specific register functions
  - Supports both MII and the reduced pin count RMII interfaces
- Power and I/Os
  - Various low power modes
  - Integrated power-on reset circuit
  - Two status LED outputs
  - Latch-Up Performance Exceeds 150mA per EIA/JESD 78, Class II
  - May be used with a single 3.3V supply
- Additional Features
  - Ability to use a low cost 25Mhz crystal for reduced BOM
- Packaging
  - 32-pin QFN/SQFN (5x5 mm) Lead-Free RoHS Compliant package with MII and RMII
- Environmental
  - Extended commercial temperature range (0°C to +85°C)
  - Industrial temperature range version available (-40°C to +85°C)

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1.0 INTRODUCTION

1.1 General Terms and Conventions

The following is list of the general terms used throughout this document:

BYTE	8-bits
FIFO	First In First Out buffer; often used for elasticity buffer
MAC	Media Access Controller
MII	Media Independent Interface
RMII™	Reduced Media Independent Interface™
N/A	Not Applicable
X	Indicates that a logic state is “don’t care” or undefined.
RESERVED	Refers to a reserved bit field or address. Unless otherwise noted, reserved bits must always be zero for write operations. Unless otherwise noted, values are not guaranteed when reading reserved bits. Unless otherwise noted, do not read or write to reserved addresses.
SMI	Serial Management Interface

1.2 General Description

The LAN8710A/LAN8710Ai is a low-power 10BASE-T/100BASE-TX physical layer (PHY) transceiver with variable I/O voltage that is compliant with the IEEE 802.3-2005 standards.

The LAN8710A/LAN8710Ai supports communication with an Ethernet MAC via a standard MII (IEEE 802.3u)/RMII interface. It contains a full-duplex 10-BASE-T/100BASE-TX transceiver and supports 10Mbps (10BASE-T) and 100Mbps (100BASE-TX) operation. The LAN8710A/LAN8710Ai implements auto-negotiation to automatically determine the best possible speed and duplex mode of operation. HP Auto-MDIX support allows the use of direct connect or cross-over LAN cables.

The LAN8710A/LAN8710Ai supports both IEEE 802.3-2005 compliant and vendor-specific register functions. However, no register access is required for operation. The initial configuration may be selected via the configuration pins as described in Section 3.7, "Configuration Straps," on page 29. Register-selectable configuration options may be used to further define the functionality of the transceiver.

Per IEEE 802.3-2005 standards, all digital interface pins are tolerant to 3.6V. The device can be configured to operate on a single 3.3V supply utilizing an integrated 3.3V to 1.2V linear regulator. The linear regulator may be optionally disabled, allowing usage of a high efficiency external regulator for lower system power dissipation.

The LAN8710A/LAN8710Ai is available in both extended commercial and industrial temperature range versions. A typical system application is shown in Figure 1-1.

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FIGURE 1-1: SYSTEM BLOCK DIAGRAM

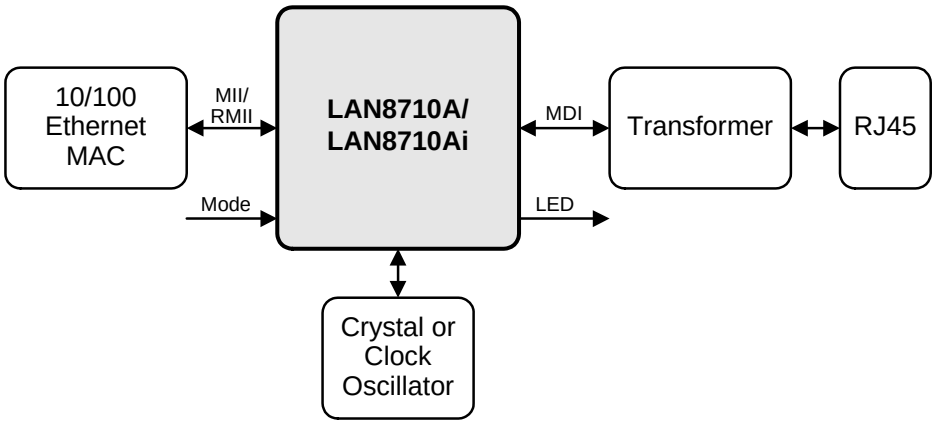
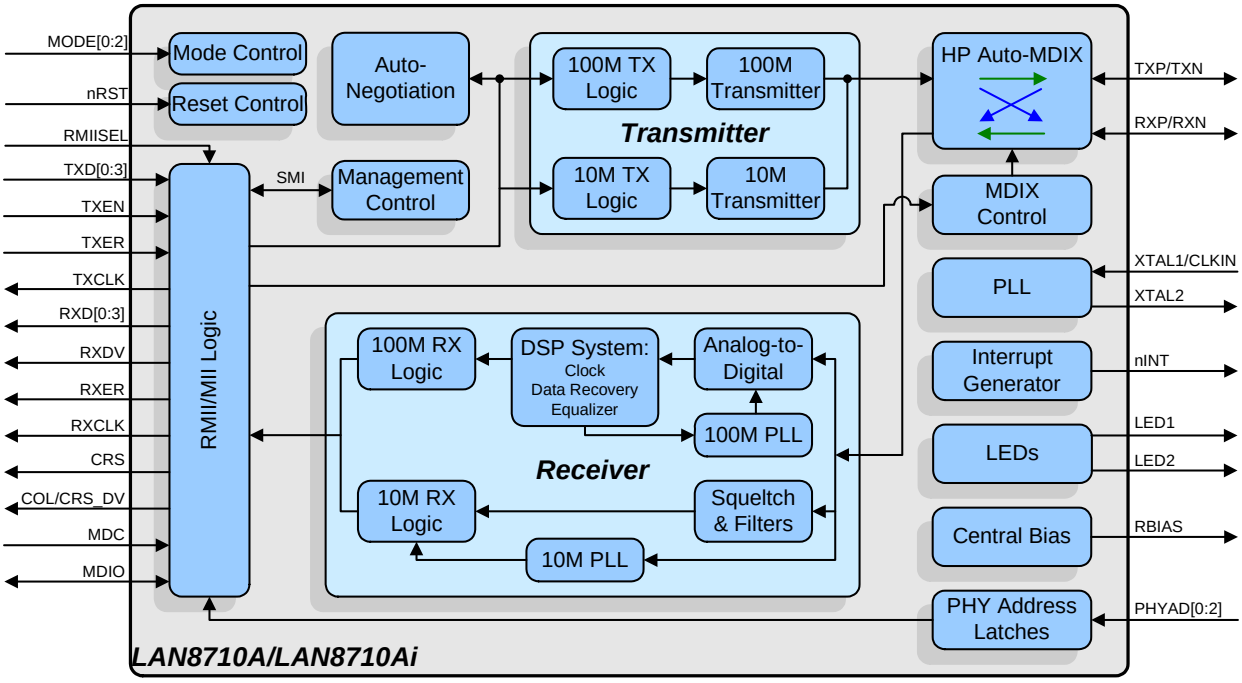
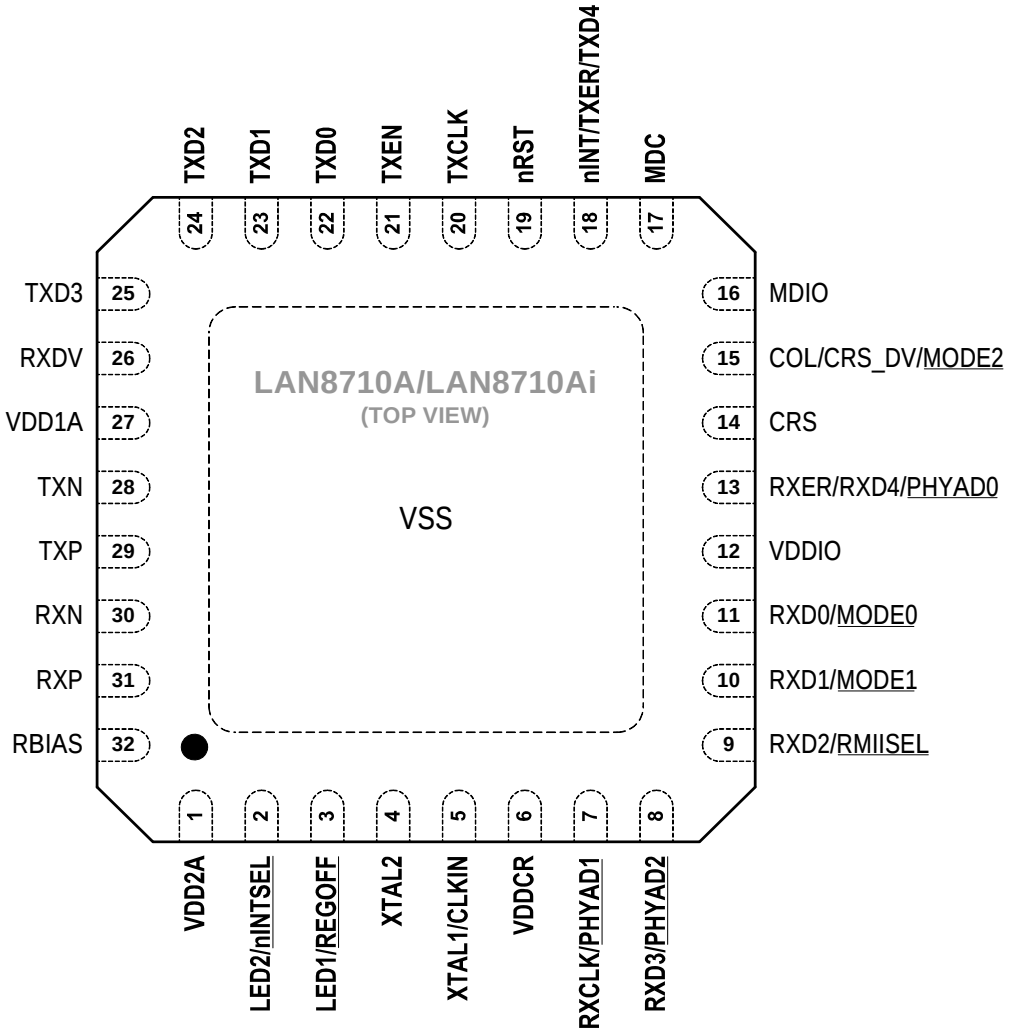


FIGURE 1-2: ARCHITECTURAL OVERVIEW



2.0 PIN DESCRIPTION AND CONFIGURATION

FIGURE 2-1: 32-QFN/SQFN PIN ASSIGNMENTS (TOP VIEW)



NOTE: Exposed pad (VSS) on bottom of package must be connected to ground

Note 2-1 When a lower case “n” is used at the beginning of the signal name, it indicates that the signal is active low. For example, nRST indicates that the reset signal is active low.

Note 2-2 The buffer type for each signal is indicated in the BUFFER TYPE column. A description of the buffer types is provided in Section 2.2.

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TABLE 2-1: MII/RMII SIGNALS

Num Pins	Name	Symbol	Buffer Type	Description
1	Transmit Data 0	TXD0	VIS	The MAC transmits data to the transceiver using this signal in all modes.
1	Transmit Data 1	TXD1	VIS	The MAC transmits data to the transceiver using this signal in all modes.
1	Transmit Data 2 (MII Mode)	TXD2	VIS	The MAC transmits data to the transceiver using this signal in MII Mode. **Note:** This signal must be grounded in RMII Mode.
1	Transmit Data 3 (MII Mode)	TXD3	VIS	The MAC transmits data to the transceiver using this signal in MII Mode. **Note:** This signal must be grounded in RMII Mode.
1	Interrupt Output	nINT	VO8	Active low interrupt output. Place an external resistor pull-up to VDDIO. **Note:** Refer to Section 3.6, "Interrupt Management," on page 27 for additional details on device interrupts. **Note:** Refer to Section 3.8.1.2, "nINTSEL and LED2 Polarity Selection," on page 33 for details on how the nINTSEL configuration strap is used to determine the function of this pin.
	Transmit Error (MII Mode)	TXER	VIS (PU)	When driven high, the 4B/5B encode process substitutes the Transmit Error code-group (/H/) for the encoded data word. This input is ignored in the 10BASE-T mode of operation.
	Transmit Data 4 (MII Mode)	TXD4	VIS (PU)	In Symbol Interface (5B Decoding) mode, this signal becomes the MII Transmit Data 4 line (the MSB of the 5-bit symbol code-group). **Note:** This signal is not used in RMII Mode.
1	Transmit Enable	TXEN	VIS (PD)	Indicates that valid transmission data is present on TXD[3:0]. In RMII Mode, only TXD[1:0] provide valid data.
1	Transmit Clock (MII Mode)	TXCLK	VO8	Used to latch data from the MAC into the transceiver. • MII (100BASE-TX): 25MHz • MII (10BASE-T): 2.5MHz **Note:** This signal is not used in RMII Mode.

TABLE 2-1: MII/RMII SIGNALS (CONTINUED)

Num Pins	Name	Symbol	Buffer Type	Description
1	Receive Data 0	RXD0	VO8	Bit 0 of the 4 (2 in RMII Mode) data bits that are sent by the transceiver on the receive path.
	PHY Operating Mode 0 Configuration Strap	MODE0	VIS (PU)	Combined with MODE1 and MODE2, this configuration strap sets the default PHY mode. See Note 2-3 for more information on configuration straps. **Note:** Refer to Section 3.7.2, "MODE[2:0]: Mode Configuration," on page 30 for additional details.
1	Receive Data 1	RXD1	VO8	Bit 1 of the 4 (2 in RMII Mode) data bits that are sent by the transceiver on the receive path.
	PHY Operating Mode 1 Configuration Strap	MODE1	VIS (PU)	Combined with MODE0 and MODE2, this configuration strap sets the default PHY mode. See Note 2-3 for more information on configuration straps. **Note:** Refer to Section 3.7.2, "MODE[2:0]: Mode Configuration," on page 30 for additional details.
1	Receive Data 2 (MII Mode)	RXD2	VO8	Bit 2 of the 4 (in MII Mode) data bits that are sent by the transceiver on the receive path. **Note:** This signal is not used in RMII Mode.
	MII/RMII Mode Select Configuration Strap	RMIISEL	VIS (PD)	This configuration strap selects the MII or RMII mode of operation. When strapped low to VSS, MII Mode is selected. When strapped high to VDDIO RMII Mode is selected. See Note 2-3 for more information on configuration straps. **Note:** Refer to Section 3.7.3, "RMIISEL: MII/RMII Mode Configuration," on page 31 for additional details.
1	Receive Data 3 (MII Mode)	RXD3	VO8	Bit 3 of the 4 (in MII Mode) data bits that are sent by the transceiver on the receive path. **Note:** This signal is not used in RMII Mode.
	PHY Address 2 Configuration Strap	PHYAD2	VIS (PD)	Combined with PHYAD0 and PHYAD1, this configuration strap sets the transceiver's SMI address. See Note 2-3 for more information on configuration straps. **Note:** Refer to Section 3.7.1, "PHYAD[2:0]: PHY Address Configuration," on page 29 for additional information.

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TABLE 2-1: MII/RMII SIGNALS (CONTINUED)

Num Pins	Name	Symbol	Buffer Type	Description
1	Receive Error	RXER	VO8	This signal is asserted to indicate that an error was detected somewhere in the frame presently being transferred from the transceiver. **Note:** This signal is optional in RMII Mode.
	Receive Data 4 (MII Mode)	RXD4	VO8	In Symbol Interface (5B Decoding) mode, this signal is the MII Receive Data 4 signal, the MSB of the received 5-bit symbol code-group. **Note:** Unless configured to the Symbol Interface mode, this pin functions as RXER.
	PHY Address 0 Configuration Strap	PHYAD0	VIS (PD)	Combined with PHYAD1 and PHYAD2, this configuration strap sets the transceiver's SMI address. See Note 2-3 for more information on configuration straps. **Note:** Refer to Section 3.7.1, "PHYAD[2:0]: PHY Address Configuration," on page 29 for additional information.
1	Receive Clock (MII Mode)	RXCLK	VO8	In MII mode, this pin is the receive clock output. • MII (100BASE-TX): 25MHz • MII (10BASE-T): 2.5MHz
	PHY Address 1 Configuration Strap	PHYAD1	VIS (PD)	Combined with PHYAD0 and PHYAD2, this configuration strap sets the transceiver's SMI address. See Note 2-3 for more information on configuration straps. **Note:** Refer to Section 3.7.1, "PHYAD[2:0]: PHY Address Configuration," on page 29 for additional information.
1	Receive Data Valid	RXDV	VO8	Indicates that recovered and decoded data is available on the RXD pins.

TABLE 2-1: MII/RMII SIGNALS (CONTINUED)

Num Pins	Name	Symbol	Buffer Type	Description
1	Carrier Sense / Receive Data Valid (RMII Mode)	CRS_DV	VO8	This signal is asserted to indicate the receive medium is non-idle in RMII Mode. When a 10BASE-T packet is received, CRS_DV is asserted, but RXD[1:0] is held low until the SFD byte (10101011) is received. **Note:** Per the RMII standard, transmitted data is not looped back onto the receive data pins in 10BASE-T half-duplex mode.
	Collision Detect (MII Mode)	COL	VO8	This signal is asserted to indicate detection of a collision condition in MII Mode.
	PHY Operating Mode 2 Configuration Strap	MODE2	VIS (PU)	Combined with MODE0 and MODE1, this configuration strap sets the default PHY mode. See Note 2-3 for more information on configuration straps. **Note:** Refer to Section 3.7.2, "MODE[2:0]: Mode Configuration," on page 30 for additional details.
1	Carrier Sense (MII Mode)	CRS	VO8 (PD)	This signal indicates detection of a carrier in MII Mode.

Note 2-3 Configuration strap values are latched on power-on reset and system reset. Configuration straps are identified by an underlined symbol name. Signals that function as configuration straps must be augmented with an external resistor when connected to a load. Refer to Section 3.7, "Configuration Straps," on page 29 for additional information.

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TABLE 2-2: LED PINS

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	LED 1	LED1	O12	Link activity LED Indication. This pin is driven active when a valid link is detected and blinks when activity is detected. **Note:** Refer to Section 3.8.1, "LEDs," on page 32 for additional LED information.
	Regulator Off Configuration Strap	REGOFF	IS (PD)	This configuration strap is used to disable the internal 1.2V regulator. When the regulator is disabled, external 1.2V must be supplied to VDDCR. • When REGOFF is pulled high to VDD2A with an external resistor, the internal regulator is disabled. • When REGOFF is floating or pulled low, the internal regulator is enabled (default). See Note 2-4 for more information on configuration straps. **Note:** Refer to Section 3.7.4, "REGOFF: Internal +1.2V Regulator Configuration," on page 32 for additional details.
1	LED 2	LED2	O12	Link Speed LED Indication. This pin is driven active when the operating speed is 100Mbps. It is inactive when the operating speed is 10Mbps or during line isolation. **Note:** Refer to Section 3.8.1, "LEDs," on page 32 for additional LED information.
	nINT/TXER/ TXD4 Function Select Configuration Strap	nINTSEL	IS (PU)	This configuration strap selects the mode of the nINT/TXER/TXD4 pin. • When nINTSEL is floated or pulled to VDD2A, nINT is selected for operation on the nINT/TXER/TXD4 pin (default). • When nINTSEL is pulled low to VSS, TXER/ TXD4 is selected for operation on the nINT/ TXER/TXD4 pin. See Note 2-4 for more information on configuration straps. **Note:** Refer to See Section 3.8.1.2, "nINTSEL and LED2 Polarity Selection," on page 33 for additional information.

Note 2-4 Configuration strap values are latched on power-on reset and system reset. Configuration straps are identified by an underlined symbol name. Signals that function as configuration straps must be augmented with an external resistor when connected to a load. Refer to Section 3.7, "Configuration Straps," on page 29 for additional information.

TABLE 2-3: SERIAL MANAGEMENT INTERFACE (SMI) PINS

Num PINs	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	SMI Data Input/Output	MDIO	VIS/ VOD8	Serial Management Interface data input/output
1	SMI Clock	MDC	VIS	Serial Management Interface clock

TABLE 2-4: ETHERNET PINS

Num PINs	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	Ethernet TX/ RX Positive Channel 1	TXP	AIO	Transmit/Receive Positive Channel 1
1	Ethernet TX/ RX Negative Channel 1	TXN	AIO	Transmit/Receive Negative Channel 1
1	Ethernet TX/ RX Positive Channel 2	RXP	AIO	Transmit/Receive Positive Channel 2
1	Ethernet TX/ RX Negative Channel 2	RXN	AIO	Transmit/Receive Negative Channel 2

TABLE 2-5: MISCELLANEOUS PINS

Num PINs	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	External Crystal Input	XTAL1	ICLK	External crystal input
	External Clock Input	CLKIN	ICLK	Single-ended clock oscillator input. **Note:** When using a single ended clock oscillator, XTAL2 should be left unconnected.
1	External Crystal Out-put	XTAL2	OCLK	External crystal output
1	External Reset	nRST	VIS (PU)	System reset. This signal is active low.

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TABLE 2-6: ANALOG REFERENCE PINS

Num PINs	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	External 1% Bias Resistor Input	RBIAS	AI	This pin requires connection of a 12.1k ohm (1%) resistor to ground. Refer to the LAN8710A/LAN8710Ai reference schematic for connection information. **Note:** The nominal voltage is 1.2V and the resistor will dissipate approximately 1mW of power.

TABLE 2-7: POWER PINS

Num PINs	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	+1.6V to +3.6V Variable I/O Power	VDDIO	P	+1.6V to +3.6V variable I/O power Refer to the LAN8710A/LAN8710Ai reference schematic for connection information.
1	+1.2V Digital Core Power Supply	VDDCR	P	Supplied by the on-chip regulator unless configured for regulator off mode via the REGOFF configuration strap. Refer to the LAN8710A/LAN8710Ai reference schematic for connection information. **Note:** 1 uF and 470 pF decoupling capacitors in parallel to ground should be used on this pin.
1	+3.3V Channel 1 Analog Port Power	VDD1A	P	+3.3V Analog Port Power to Channel 1 Refer to the LAN8710A/LAN8710Ai reference schematic for connection information.
1	+3.3V Channel 2 Analog Port Power	VDD2A	P	+3.3V Analog Port Power to Channel 2 and the internal regulator. Refer to the LAN8710A/LAN8710Ai reference schematic for connection information.
1	Ground	VSS	P	Common ground. This exposed pad must be connected to the ground plane with a via array.

2.1 Pin Assignments

TABLE 2-8: 32-QFN PACKAGE PIN ASSIGNMENTS

Pin NUM	Pin Name	Pin NUM	Pin Name
1	VDD2A	17	MDC
2	LED2/nINTSEL	18	nINT/TXER/TXD4
3	LED1/REGOFF	19	nRST
4	XTAL2	20	TXCLK
5	XTAL1/CLKIN	21	TXEN
6	VDDCR	22	TXD0
7	RXCLK/PHYAD1	23	TXD1
8	RXD3/PHYAD2	24	TXD2
9	RXD2/RMIISEL	25	TXD3
10	RXD1/MODE1	26	RXDV
11	RXD0/MODE0	27	VDD1A
12	VDDIO	28	TXN
13	RXER/RXD4/PHYAD0	29	TXP
14	CRS	30	RXN
15	COL/CRS_DV/MODE2	31	RXP
16	MDIO	32	RBIAS

2.2 Buffer Types

TABLE 2-9: BUFFER TYPES

BUFFER TYPE	DESCRIPTION
IS	Schmitt-triggered input
O12	Output with 12mA sink and 12mA source
VIS	Variable voltage Schmitt-triggered input
VO8	Variable voltage output with 8mA sink and 8mA source
VOD8	Variable voltage open-drain output with 8mA sink
PU	50uA (typical) internal pull-up. Unless otherwise noted in the pin description, internal pull-ups are always enabled. **Note:** Internal pull-up resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled high, an external resistor must be added.

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TABLE 2-9: BUFFER TYPES (CONTINUED)

BUFFER TYPE	DESCRIPTION
PD	50uA (typical) internal pull-down. Unless otherwise noted in the pin description, internal pull-downs are always enabled. **Note:** Internal pull-down resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled low, an external resistor must be added.
AI	Analog input
AIO	Analog bi-directional
ICLK	Crystal oscillator input pin
OCLK	Crystal oscillator output pin
P	Power pin

Note 2-5 The digital signals are not 5V tolerant. Refer to Section 5.1, "Absolute Maximum Ratings*," on page 54 for additional buffer information.

Note 2-6 Sink and source capabilities are dependent on the VDDIO voltage. Refer to Section 5.1, "Absolute Maximum Ratings*," on page 54 for additional information.

3.0 FUNCTIONAL DESCRIPTION

This chapter provides functional descriptions of the various device features. These features have been categorized into the following sections:

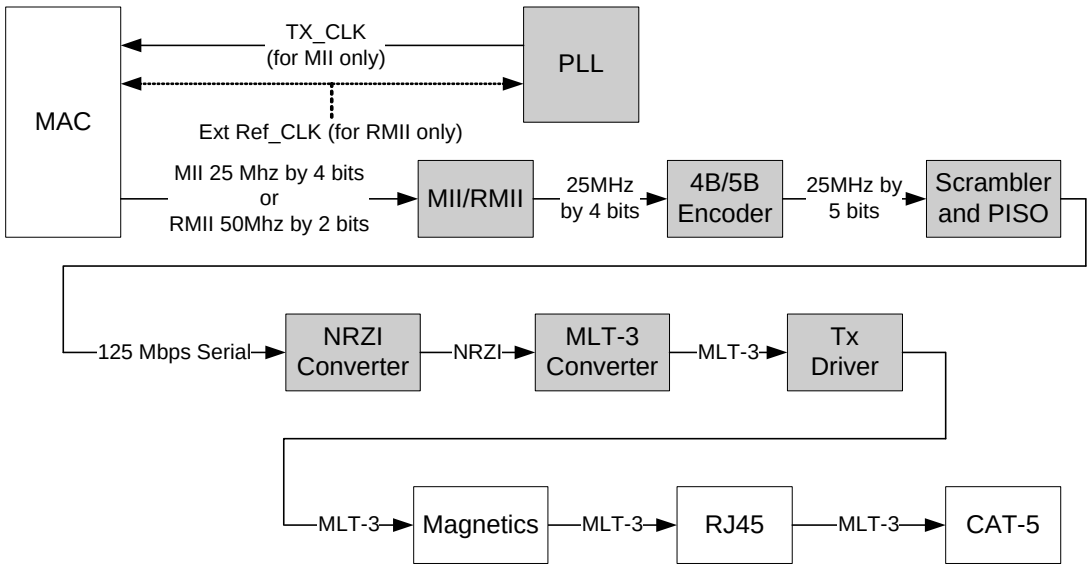
- Transceiver
- Auto-negotiation
- HP Auto-MDIX Support
- MAC Interface
- Serial Management Interface (SMI)
- Interrupt Management
- Configuration Straps
- Miscellaneous Functions
- Application Diagrams

3.1 Transceiver

3.1.1 100BASE-TX TRANSMIT

The 100BASE-TX transmit data path is shown in Figure 3-1. Each major block is explained in the following subsections.

FIGURE 3-1: 100BASE-TX TRANSMIT DATA PATH



3.1.1.1 100BASE-TX Transmit Data Across the MII/RMII Interface

For MII, the MAC controller drives the transmit data onto the TXD bus and asserts TXEN to indicate valid data. The data is latched by the transceiver's MII block on the rising edge of TXCLK. The data is in the form of 4-bit wide 25MHz data.

For RMII, the MAC controller drives the transmit data onto the TXD bus and asserts TXEN to indicate valid data. The data is latched by the transceiver's RMII block on the rising edge of REF_CLK. The data is in the form of 2-bit wide 50MHz data.

3.1.1.2 4B/5B Encoding

The transmit data passes from the MII/RMII block to the 4B/5B encoder. This block encodes the data from 4-bit nibbles to 5-bit symbols (known as "code-groups") according to Table 3-1. Each 4-bit data-nibble is mapped to 16 of the 32 possible code-groups. The remaining 16 code-groups are either used for control information or are not valid.

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The first 16 code-groups are referred to by the hexadecimal values of their corresponding data nibbles, 0 through F. The remaining code-groups are given letter designations with slashes on either side. For example, an IDLE code-group is /I/, a transmit error code-group is /H/, etc.

TABLE 3-1: 4B/5B CODE TABLE

CODE GROUP	SYM	RECEIVER INTERPRETATION			TRANSMITTER INTERPRETATION		
11110	0	0	0000	DATA	0	0000	DATA
01001	1	1	0001	—	1	0001	—
10100	2	2	0010	—	2	0010	—
10101	3	3	0011	—	3	0011	—
01010	4	4	0100	—	4	0100	—
01011	5	5	0101	—	5	0101	—
01110	6	6	0110	—	6	0110	—
01111	7	7	0111	—	7	0111	—
10010	8	8	1000	—	8	1000	—
10011	9	9	1001	—	9	1001	—
10110	A	A	1010	—	A	1010	—
10111	B	B	1011	—	B	1011	—
11010	C	C	1100	—	C	1100	—
11011	D	D	1101	—	D	1101	—
11100	E	E	1110	—	E	1110	—
11101	F	F	1111	—	F	1111	—
11111	I	IDLE			Sent after /T/R until TXEN		
11000	J	First nibble of SSD, translated to “0101” following IDLE, else RXER			Sent for rising TXEN		
10001	K	Second nibble of SSD, translated to “0101” following J, else RXER			Sent for rising TXEN		
01101	T	First nibble of ESD, causes de-assertion of CRS if followed by /R/, else assertion of RXER			Sent for falling TXEN		
00111	R	Second nibble of ESD, causes deassertion of CRS if following /T/, else assertion of RXER			Sent for falling TXEN		
00100	H	Transmit Error Symbol			Sent for rising TXER		
00110	V	INVALID, RXER if during RXDV			INVALID		
11001	V	INVALID, RXER if during RXDV			INVALID		
00000	V	INVALID, RXER if during RXDV			INVALID		
00001	V	INVALID, RXER if during RXDV			INVALID		

TABLE 3-1: 4B/5B CODE TABLE (CONTINUED)

CODE GROUP	SYM	RECEIVER INTERPRETATION	TRANSMITTER INTERPRETATION
00010	V	INVALID, RXER if during RXDV	INVALID
00011	V	INVALID, RXER if during RXDV	INVALID
00101	V	INVALID, RXER if during RXDV	INVALID
01000	V	INVALID, RXER if during RXDV	INVALID
01100	V	INVALID, RXER if during RXDV	INVALID
10000	V	INVALID, RXER if during RXDV	INVALID

3.1.1.3 Scrambling

Repeated data patterns (especially the IDLE code-group) can have power spectral densities with large narrow-band peaks. Scrambling the data helps eliminate these peaks and spread the signal power more uniformly over the entire channel bandwidth. This uniform spectral density is required by FCC regulations to prevent excessive EMI from being radiated by the physical wiring.

The seed for the scrambler is generated from the transceiver address, PHYAD, ensuring that in multiple-transceiver applications, such as repeaters or switches, each transceiver will have its own scrambler sequence.

The scrambler also performs the Parallel In Serial Out conversion (PISO) of the data.

3.1.1.4 NRZI and MLT-3 Encoding

The scrambler block passes the 5-bit wide parallel data to the NRZI converter where it becomes a serial 125MHz NRZI data stream. The NRZI is encoded to MLT-3. MLT-3 is a tri-level code where a change in the logic level represents a code bit “1” and the logic output remaining at the same level represents a code bit “0”.

3.1.1.5 100M Transmit Driver

The MLT3 data is then passed to the analog transmitter, which drives the differential MLT-3 signal, on outputs TXP and TXN, to the twisted pair media across a 1:1 ratio isolation transformer. The 10BASE-T and 100BASE-TX signals pass through the same transformer so that common “magnetics” can be used for both. The transmitter drives into the 100Ω impedance of the CAT-5 cable. Cable termination and impedance matching require external components.

3.1.1.6 100M Phase Lock Loop (PLL)

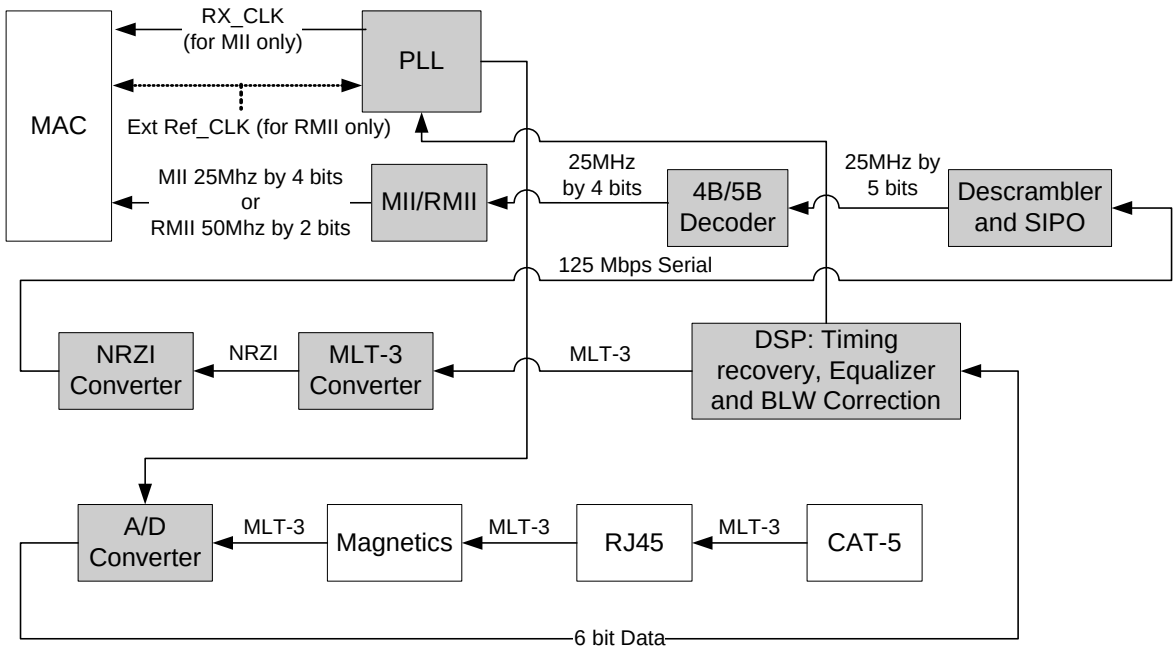
The 100M PLL locks onto reference clock and generates the 125MHz clock used to drive the 125 MHz logic and the 100BASE-TX transmitter.

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3.1.2 100BASE-TX RECEIVE

The 100BASE-TX receive data path is shown in Figure 3-2. Each major block is explained in the following subsections.

FIGURE 3-2: 100BASE-TX RECEIVE DATA PATH



3.1.2.1 100M Receive Input

The MLT-3 from the cable is fed into the transceiver (on inputs RXP and RXN) via a 1:1 ratio transformer. The ADC samples the incoming differential signal at a rate of 125M samples per second. Using a 64-level quanitizer, it generates 6 digital bits to represent each sample. The DSP adjusts the gain of the ADC according to the observed signal levels such that the full dynamic range of the ADC can be used.

3.1.2.2 Equalizer, Baseline Wander Correction and Clock and Data Recovery

The 6 bits from the ADC are fed into the DSP block. The equalizer in the DSP section compensates for phase and amplitude distortion caused by the physical channel consisting of magnetics, connectors, and CAT- 5 cable. The equalizer can restore the signal for any good-quality CAT-5 cable between 1m and 150m.

If the DC content of the signal is such that the low-frequency components fall below the low frequency pole of the isolation transformer, then the droop characteristics of the transformer will become significant and Baseline Wander (BLW) on the received signal will result. To prevent corruption of the received data, the transceiver corrects for BLW and can receive the ANSI X3.263-1995 FDDI TP-PMD defined “killer packet” with no bit errors.

The 100M PLL generates multiple phases of the 125MHz clock. A multiplexer, controlled by the timing unit of the DSP, selects the optimum phase for sampling the data. This is used as the received recovered clock. This clock is used to extract the serial data from the received signal.

3.1.2.3 NRZI and MLT-3 Decoding

The DSP generates the MLT-3 recovered levels that are fed to the MLT-3 converter. The MLT-3 is then converted to an NRZI data stream.

3.1.2.4 Descrambling

The descrambler performs an inverse function to the scrambler in the transmitter and also performs the Serial In Parallel Out (SIPO) conversion of the data.

During reception of IDLE (/I/) symbols. the descrambler synchronizes its descrambler key to the incoming stream. Once synchronization is achieved, the descrambler locks on this key and is able to descramble incoming data.

Special logic in the descrambler ensures synchronization with the remote transceiver by searching for IDLE symbols within a window of 4000 bytes (40us). This window ensures that a maximum packet size of 1514 bytes, allowed by the IEEE 802.3 standard, can be received with no interference. If no IDLE-symbols are detected within this time-period, receive operation is aborted and the descrambler re-starts the synchronization process.

3.1.2.5 Alignment

The de-scrambled signal is then aligned into 5-bit code-groups by recognizing the /J/K/ Start-of-Stream Delimiter (SSD) pair at the start of a packet. Once the code-word alignment is determined, it is stored and utilized until the next start of frame.

3.1.2.6 5B/4B Decoding

The 5-bit code-groups are translated into 4-bit data nibbles according to the 4B/5B table. The translated data is presented on the RXD[3:0] signal lines. The SSD, /J/K/, is translated to “0101 0101” as the first 2 nibbles of the MAC preamble. Reception of the SSD causes the transceiver to assert the receive data valid signal, indicating that valid data is available on the RXD bus. Successive valid code-groups are translated to data nibbles. Reception of either the End of Stream Delimiter (ESD) consisting of the /T/R/ symbols, or at least two /I/ symbols causes the transceiver to de-assert the carrier sense and receive data valid signals.

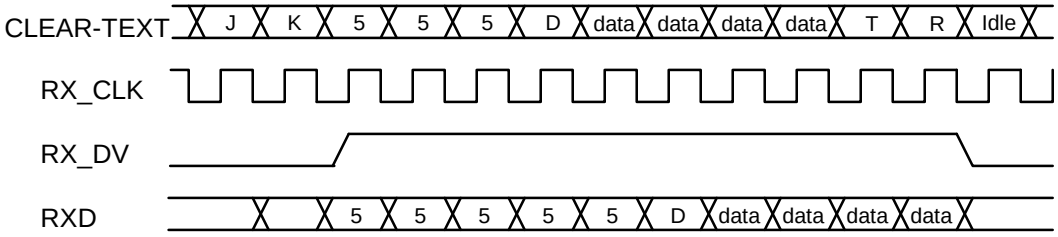
Note: These symbols are not translated into data.

3.1.2.7 Receive Data Valid Signal

The Receive Data Valid signal (RXDV) indicates that recovered and decoded nibbles are being presented on the RXD[3:0] outputs synchronous to RXCLK. RXDV becomes active after the /J/K/ delimiter has been recognized and RXD is aligned to nibble boundaries. It remains active until either the /T/R/ delimiter is recognized or link test indicates failure or SIGDET becomes false.

RXDV is asserted when the first nibble of translated /J/K/ is ready for transfer over the Media Independent Interface (MII mode).

FIGURE 3-3: RELATIONSHIP BETWEEN RECEIVED DATA AND SPECIFIC MII SIGNALS



3.1.2.8 Receiver Errors

During a frame, unexpected code-groups are considered receive errors. Expected code groups are the DATA set (0 through F), and the /T/R/ (ESD) symbol pair. When a receive error occurs, the RXER signal is asserted and arbitrary data is driven onto the RXD[3:0] lines. Should an error be detected during the time that the /J/K/ delimiter is being decoded (bad SSD error), RXER is asserted true and the value ‘1110’ is driven onto the RXD[3:0] lines. Note that the Valid Data signal is not yet asserted when the bad SSD error occurs.

3.1.2.9 100M Receive Data Across the MII/RMII Interface

In MII mode, the 4-bit data nibbles are sent to the MII block. These data nibbles are clocked to the controller at a rate of 25MHz. The controller samples the data on the rising edge of RXCLK. To ensure that the setup and hold requirements are met, the nibbles are clocked out of the transceiver on the falling edge of RXCLK. RXCLK is the 25MHz output clock for the MII bus. It is recovered from the received data to clock the RXD bus. If there is no received signal, it is derived from the system reference clock (XTAL1/CLKIN).

When tracking the received data, RXCLK has a maximum jitter of 0.8ns (provided that the jitter of the input clock, XTAL1/CLKIN, is below 100ps).

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In RMII mode, the 2-bit data nibbles are sent to the RMII block. These data nibbles are clocked to the controller at a rate of 50MHz. The controller samples the data on the rising edge of XTAL1/CLKIN (REF_CLK). To ensure that the setup and hold requirements are met, the nibbles are clocked out of the transceiver on the falling edge of XTAL1/CLKIN (REF_CLK).

3.1.3 10BASE-T TRANSMIT

Data to be transmitted comes from the MAC layer controller. The 10BASE-T transmitter receives 4-bit nibbles from the MII at a rate of 2.5MHz and converts them to a 10Mbps serial data stream. The data stream is then Manchester-encoded and sent to the analog transmitter, which drives a signal onto the twisted pair via the external magnetics.

The 10M transmitter uses the following blocks:

- MII (digital)
- TX 10M (digital)
- 10M Transmitter (analog)
- 10M PLL (analog)

3.1.3.1 10M Transmit Data Across the MII/RMII Interface

The MAC controller drives the transmit data onto the TXD bus. For MII, when the controller has driven TXEN high to indicate valid data, the data is latched by the MII block on the rising edge of TXCLK. The data is in the form of 4-bit wide 2.5MHz data. For RMII, TXD[1:0] shall transition synchronously with respect to REF_CLK. When TXEN is asserted, TXD[1:0] are accepted for transmission by the device. TXD[1:0] shall be “00” to indicate idle when TXEN is deasserted. Values of TXD[1:0] other than “00” when TXEN is deasserted are reserved for out-of-band signaling (to be defined). Values other than “00” on TXD[1:0] while TXEN is deasserted shall be ignored by the device.TXD[1:0] shall provide valid data for each REF_CLK period while TXEN is asserted.

In order to comply with legacy 10BASE-T MAC/Controllers, in half-duplex mode the transceiver loops back the transmitted data, on the receive path. This does not confuse the MAC/Controller since the COL signal is not asserted during this time. The transceiver also supports the SQE (Heartbeat) signal. See Section 3.8.7, "Collision Detect," on page 35, for more details.

3.1.3.2 Manchester Encoding

The 4-bit wide data is sent to the 10M TX block. The nibbles are converted to a 10Mbps serial NRZI data stream. The 10M PLL locks onto the external clock or internal oscillator and produces a 20MHz clock. This is used to Manchester encode the NRZ data stream. When no data is being transmitted (TXEN is low), the 10M TX block outputs Normal Link Pulses (NLPs) to maintain communications with the remote link partner.

3.1.3.3 10M Transmit Drivers

The Manchester encoded data is sent to the analog transmitter where it is shaped and filtered before being driven out as a differential signal across the TXP and TXN outputs.

3.1.4 10BASE-T RECEIVE

The 10BASE-T receiver gets the Manchester- encoded analog signal from the cable via the magnetics. It recovers the receive clock from the signal and uses this clock to recover the NRZI data stream. This 10M serial data is converted to 4-bit data nibbles which are passed to the controller via MII at a rate of 2.5MHz.

This 10M receiver uses the following blocks:

- Filter and SQUELCH (analog)
- 10M PLL (analog)
- RX 10M (digital)
- MII (digital)

3.1.4.1 10M Receive Input and Squelch

The Manchester signal from the cable is fed into the transceiver (on inputs RXP and RXN) via 1:1 ratio magnetics. It is first filtered to reduce any out-of-band noise. It then passes through a SQUELCH circuit. The SQUELCH is a set of amplitude and timing comparators that normally reject differential voltage levels below 300mV and detect and recognize differential voltages above 585mV.

3.1.4.2 Manchester Decoding

The output of the SQUELCH goes to the 10M RX block where it is validated as Manchester encoded data. The polarity of the signal is also checked. If the polarity is reversed (local RXP is connected to RXN of the remote partner and vice versa), the condition is identified and corrected. The reversed condition is indicated by the XPOL bit of the Special Control/Status Indications Register. The 10M PLL is locked onto the received Manchester signal, from which the 20MHz cock is generated. Using this clock, the Manchester encoded data is extracted and converted to a 10MHz NRZI data stream. It is then converted from serial to 4-bit wide parallel data.

The 10M RX block also detects valid 10Base-T IDLE signals - Normal Link Pulses (NLPs) - to maintain the link.

3.1.4.3 10M Receive Data Across the MII/RMII Interface

For MII, the 4-bit data nibbles are sent to the MII block. In MII mode, these data nibbles are valid on the rising edge of the 2.5 MHz RXCLK.

For RMII, the 2-bit data nibbles are sent to the RMII block. In RMII mode, these data nibbles are valid on the rising edge of the RMII REF_CLK.

3.1.4.4 Jabber Detection

Jabber is a condition in which a station transmits for a period of time longer than the maximum permissible packet length, usually due to a fault condition, which results in holding the TXEN input for a long period. Special logic is used to detect the jabber state and abort the transmission to the line within 45ms. Once TXEN is deasserted, the logic resets the jabber condition.

As shown in Section 4.2.2, "Basic Status Register," on page 45, the Jabber Detect bit indicates that a jabber condition was detected.

3.2 Auto-negotiation

The purpose of the auto-negotiation function is to automatically configure the transceiver to the optimum link parameters based on the capabilities of its link partner. Auto-negotiation is a mechanism for exchanging configuration information between two link-partners and automatically selecting the highest performance mode of operation supported by both sides. Auto-negotiation is fully defined in clause 28 of the IEEE 802.3 specification.

Once auto-negotiation has completed, information about the resolved link can be passed back to the controller via the Serial Management Interface (SMI). The results of the negotiation process are reflected in the Speed Indication bits of the PHY Special Control/Status Register, as well as in the Auto Negotiation Link Partner Ability Register. The auto-negotiation protocol is a purely physical layer activity and proceeds independently of the MAC controller.

The advertised capabilities of the transceiver are stored in the Auto Negotiation Advertisement Register. The default advertised by the transceiver is determined by user-defined on-chip signal options.

The following blocks are activated during an Auto-negotiation session:

- Auto-negotiation (digital)
- 100M ADC (analog)
- 100M PLL (analog)
- 100M equalizer/BLW/clock recovery (DSP)
- 10M SQUELCH (analog)
- 10M PLL (analog)
- 10M Transmitter (analog)

When enabled, auto-negotiation is started by the occurrence of one of the following events:

- Hardware reset
- Software reset
- Power-down reset
- Link status down
- Setting the Restart Auto-Negotiate bit of the Basic Control Register

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On detection of one of these events, the transceiver begins auto-negotiation by transmitting bursts of Fast Link Pulses (FLP), which are bursts of link pulses from the 10M transmitter. They are shaped as Normal Link Pulses and can pass uncorrupted down CAT-3 or CAT-5 cable. A Fast Link Pulse Burst consists of up to 33 pulses. The 17 odd-numbered pulses, which are always present, frame the FLP burst. The 16 even-numbered pulses, which may be present or absent, contain the data word being transmitted. Presence of a data pulse represents a “1”, while absence represents a “0”.

The data transmitted by an FLP burst is known as a “Link Code Word.” These are defined fully in IEEE 802.3 clause 28. In summary, the transceiver advertises 802.3 compliance in its selector field (the first 5 bits of the Link Code Word). It advertises its technology ability according to the bits set in the Auto Negotiation Advertisement Register.

There are 4 possible matches of the technology abilities. In the order of priority these are:

- 100M Full Duplex (Highest Priority)
- 100M Half Duplex
- 10M Full Duplex
- 10M Half Duplex (Lowest Priority)

If the full capabilities of the transceiver are advertised (100M, Full Duplex), and if the link partner is capable of 10M and 100M, then auto-negotiation selects 100M as the highest performance mode. If the link partner is capable of half and full duplex modes, then auto-negotiation selects full duplex as the highest performance operation.

Once a capability match has been determined, the link code words are repeated with the acknowledge bit set. Any difference in the main content of the link code words at this time will cause auto-negotiation to re-start. Auto-negotiation will also re-start if not all of the required FLP bursts are received.

The capabilities advertised during auto-negotiation by the transceiver are initially determined by the logic levels latched on the MODE[2:0] configuration straps after reset completes. These configuration straps can also be used to disable auto-negotiation on power-up. Refer to Section 3.7.2, "MODE[2:0]: Mode Configuration," on page 30 for additional information.

Writing the bits 8 through 5 of the Auto Negotiation Advertisement Register allows software control of the capabilities advertised by the transceiver. Writing the Auto Negotiation Advertisement Register does not automatically re-start auto-negotiation. The Restart Auto-Negotiate bit of the Basic Control Register must be set before the new abilities will be advertised. Auto-negotiation can also be disabled via software by clearing the Auto-Negotiation Enable bit of the Basic Control Register.

Note: The device does not support “Next Page” capability.

3.2.1 PARALLEL DETECTION

If the LAN8710A/LAN8710Ai is connected to a device lacking the ability to auto-negotiate (for example, no FLPs are detected), it is able to determine the speed of the link based on either 100M MLT-3 symbols or 10M Normal Link Pulses. In this case the link is presumed to be half duplex per the IEEE standard. This ability is known as “Parallel Detection.” This feature ensures interoperability with legacy link partners. If a link is formed via parallel detection, then the Link Partner Auto-Negotiation Able bit of the Auto Negotiation Expansion Register is cleared to indicate that the Link Partner is not capable of auto-negotiation. The controller has access to this information via the management interface. If a fault occurs during parallel detection, the Parallel Detection Fault bit of Link Partner Auto-Negotiation Able is set.

Auto Negotiation Link Partner Ability Register is used to store the link partner ability information, which is coded in the received FLPs. If the link partner is not auto-negotiation capable, then the Auto Negotiation Link Partner Ability Register is updated after completion of parallel detection to reflect the speed capability of the link partner.

3.2.2 RESTARTING AUTO-NEGOTIATION

Auto-negotiation can be restarted at any time by setting the Restart Auto-Negotiate bit of the Basic Control Register. Auto-negotiation will also restart if the link is broken at any time. A broken link is caused by signal loss. This may occur because of a cable break, or because of an interruption in the signal transmitted by the link partner. Auto-negotiation resumes in an attempt to determine the new link configuration.

If the management entity re-starts auto-negotiation by setting the Restart Auto-Negotiate bit of the Basic Control Register, the LAN8710A/LAN8710Ai will respond by stopping all transmission/receiving operations. Once the break_link_timer is completed in the Auto-negotiation state-machine (approximately 1200ms), auto-negotiation will re-start. In this case, the link partner will have also dropped the link due to lack of a received signal, so it too will resume auto-negotiation.

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3.2.3 DISABLING AUTO-NEGOTIATION

Auto-negotiation can be disabled by setting the Auto-Negotiation Enable bit of the Basic Control Register to zero. The device will then force its speed of operation to reflect the information in the Basic Control Register (Speed Select bit and Duplex Mode bit). These bits should be ignored when auto-negotiation is enabled.

3.2.4 HALF VS. FULL DUPLEX

Half duplex operation relies on the CSMA/CD (Carrier Sense Multiple Access / Collision Detect) protocol to handle network traffic and collisions. In this mode, the carrier sense signal, CRS, responds to both transmit and receive activity. If data is received while the transceiver is transmitting, a collision results.

In full duplex mode, the transceiver is able to transmit and receive data simultaneously. In this mode, CRS responds only to receive activity. The CSMA/CD protocol does not apply and collision detection is disabled.

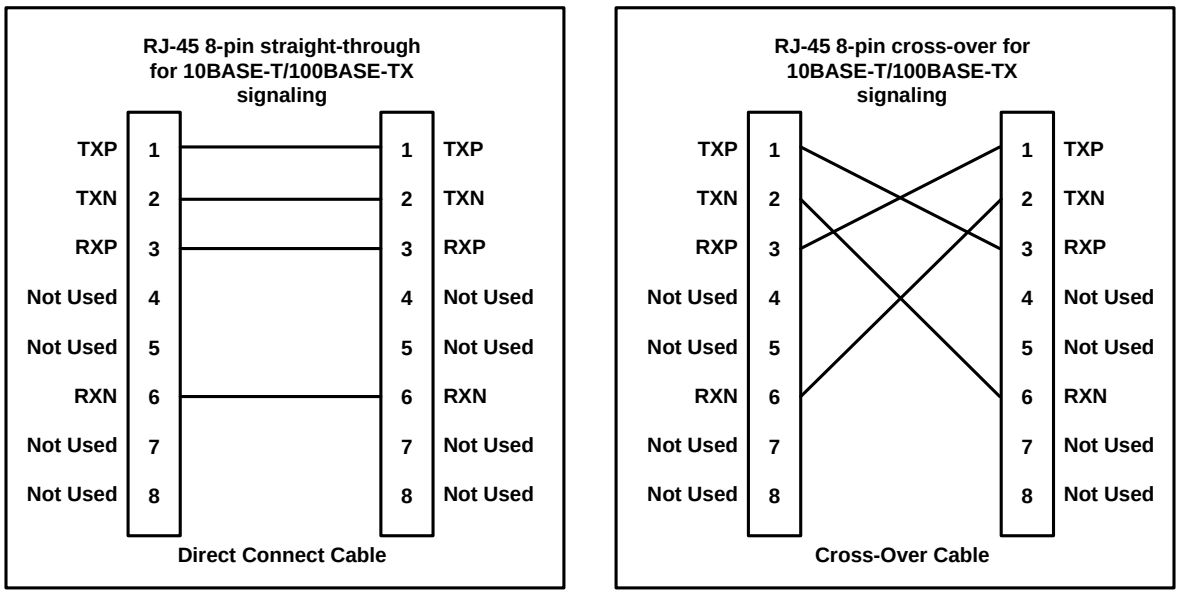
3.3 HP Auto-MDIX Support

HP Auto-MDIX facilitates the use of CAT-3 (10BASE-T) or CAT-5 (100BASE-T) media UTP interconnect cable without consideration of interface wiring scheme. If a user plugs in either a direct connect LAN cable, or a cross-over patch cable, as shown in Figure 3-4, the device's Auto-MDIX transceiver is capable of configuring the TXP/TXN and RXP/RXN pins for correct transceiver operation.

The internal logic of the device detects the TX and RX pins of the connecting device. Since the RX and TX line pairs are interchangeable, special PCB design considerations are needed to accommodate the symmetrical magnetics and termination of an Auto-MDIX design.

The Auto-MDIX function can be disabled via the AMDIXCTRL bit in the Special Control/Status Indications Register.

FIGURE 3-4: DIRECT CABLE CONNECTION VS. CROSS-OVER CABLE CONNECTION



3.4 MAC Interface

The MII/RMII block is responsible for communication with the MAC controller. Special sets of hand-shake signals are used to indicate that valid received/transmitted data is present on the 4 bit receive/transmit bus.

The device must be configured in MII or RMII mode. This is done by specific pin strapping configurations. Refer to Section 3.4.2.3, "MII vs. RMII Configuration," on page 26 for information on pin strapping and how the pins are mapped differently.

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3.4.1 MII

The MII includes 16 interface signals:

- transmit data - TXD[3:0]
- transmit strobe - TXEN
- transmit clock - TXCLK
- transmit error - TXER/TXD4
- receive data - RXD[3:0]
- receive strobe - RXDV
- receive clock - RXCLK
- receive error - RXER/RXD4/PHYAD0
- collision indication - COL
- carrier sense - CRS

In MII mode, on the transmit path, the transceiver drives the transmit clock, TXCLK, to the controller. The controller synchronizes the transmit data to the rising edge of TXCLK. The controller drives TXEN high to indicate valid transmit data. The controller drives TXER high when a transmit error is detected.

On the receive path, the transceiver drives both the receive data, RXD[3:0], and the RXCLK signal. The controller clocks in the receive data on the rising edge of RXCLK when the transceiver drives RXDV high. The transceiver drives RXER high when a receive error is detected.

3.4.2 RMII

The device supports the low pin count Reduced Media Independent Interface (RMII) intended for use between Ethernet transceivers and switch ASICs. Under IEEE 802.3, an MII comprised of 16 pins for data and control is defined. In devices incorporating many MACs or transceiver interfaces such as switches, the number of pins can add significant cost as the port counts increase. RMII reduces this pin count while retaining a management interface (MDIO/MDC) that is identical to MII.

The RMII interface has the following characteristics:

- It is capable of supporting 10Mbps and 100Mbps data rates
- A single clock reference is used for both transmit and receive
- It provides independent 2-bit (di-bit) wide transmit and receive data paths
- It uses LVCMOS signal levels, compatible with common digital CMOS ASIC processes

The RMII includes the following interface signals (1 optional):

- transmit data - TXD[1:0]
- transmit strobe - TXEN
- receive data - RXD[1:0]
- receive error - RXER (Optional)
- carrier sense - CRS_DV
- Reference Clock - (RMII references usually define this signal as REF_CLK)

3.4.2.1 CRS_DV - Carrier Sense/Receive Data Valid

The CRS_DV is asserted by the device when the receive medium is non-idle. CRS_DV is asserted asynchronously on detection of carrier due to the criteria relevant to the operating mode. In 10BASE-T mode when squelch is passed, or in 100BASE-X mode when 2 non-contiguous zeros in 10 bits are detected, the carrier is said to be detected.

Loss of carrier shall result in the deassertion of CRS_DV synchronous to the cycle of REF_CLK which presents the first di-bit of a nibble onto RXD[1:0] (for example, CRS_DV is deasserted only on nibble boundaries). If the device has additional bits to be presented on RXD[1:0] following the initial deassertion of CRS_DV, then the device shall assert CRS_DV on cycles of REF_CLK which present the second di-bit of each nibble and de-assert CRS_DV on cycles of REF_CLK which present the first di-bit of a nibble. The result is, starting on nibble boundaries, CRS_DV toggles at 25 MHz in 100Mbps mode and 2.5 MHz in 10Mbps mode when CRS ends before RXDV (for example, the FIFO still has bits to transfer when the carrier event ends). Therefore, the MAC can accurately recover RXDV and CRS.

During a false carrier event, CRS_DV shall remain asserted for the duration of carrier activity. The data on RXD[1:0] is considered valid once CRS_DV is asserted. However, since the assertion of CRS_DV is asynchronous relative to REF_CLK, the data on RXD[1:0] shall be “00” until proper receive signal decoding takes place.

3.4.2.2 Reference Clock (REF_CLK)

The RMII REF_CLK is a continuous clock that provides the timing reference for CRS_DV, RXD[1:0], TXEN, TXD[1:0] and RXER. The device uses REF_CLK as the network clock such that no buffering is required on the transmit data path. However, on the receive data path, the receiver recovers the clock from the incoming data stream, and the device uses elasticity buffering to accommodate for differences between the recovered clock and the local REF_CLK.

3.4.2.3 MII vs. RMII Configuration

The device must be configured to support the MII or RMII bus for connectivity to the MAC. This configuration is done via the RMIISEL configuration strap. MII or RMII mode selection is configured based on the strapping of the RMIISEL configuration strap as described in Section 3.7.3, "RMIISEL: MII/RMII Mode Configuration," on page 31.

Most of the MII and RMII pins are multiplexed. Table 3-2 describes the relationship of the related device pins to the MII and RMII mode signal names.

TABLE 3-2: MII/RMII SIGNAL MAPPING

PIN Name	MII Mode	RMII Mode
TXD0	TXD0	TXD0
TXD1	TXD1	TXD1
TXEN	TXEN	TXEN
RXER/ RXD4/PHYAD0	RXER	RXER Note 3-2
COL/CRS_DV/MODE2	COL	CRS_DV
RXD0/MODE0	RXD0	RXD0
RXD1/MODE1	RXD1	RXD1
TXD2	TXD2	Note 3-1
TXD3	TXD3	Note 3-1
nINT/TXER/TXD4	TXER/ TXD4	—
CRS	CRS	—
RXDV	RXDV	—
RXD2/RMIISEL	RXD2	—
RXD3/PHYAD2	RXD3	—
TXCLK	TXCLK	—
RXCLK/PHYAD1	RXCLK	—
XTAL1/CLKIN	XTAL1/CLKIN	REF_CLK

Note 3-1 In RMII mode, this pin needs to tied to VSS.

Note 3-2 The RXER signal is optional on the RMII bus. This signal is required by the transceiver, but it is optional for the MAC. The MAC can choose to ignore or not use this signal.

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3.5 Serial Management Interface (SMI)

The Serial Management Interface is used to control the device and obtain its status. This interface supports registers 0 through 6 as required by Clause 22 of the 802.3 standard, as well as “vendor-specific” registers 16 to 31 allowed by the specification. Non-supported registers (such as 7 to 15) will be read as hexadecimal “FFFF”. Device registers are detailed in Section 4.0, "Register Descriptions," on page 43.

At the system level, SMI provides 2 signals: MDIO and MDC. The MDC signal is an aperiodic clock provided by the station management controller (SMC). MDIO is a bi-directional data SMI input/output signal that receives serial data (commands) from the controller SMC and sends serial data (status) to the SMC. The minimum time between edges of the MDC is 160 ns. There is no maximum time between edges. The minimum cycle time (time between two consecutive rising or two consecutive falling edges) is 400 ns. These modest timing requirements allow this interface to be easily driven by the I/O port of a microcontroller.

The data on the MDIO line is latched on the rising edge of the MDC. The frame structure and timing of the data is shown in Figure 3-5 and Figure 3-6. The timing relationships of the MDIO signals are further described in Section 5.5.6, "SMI Timing," on page 64.

FIGURE 3-5: MDIO TIMING AND FRAME STRUCTURE - READ CYCLE

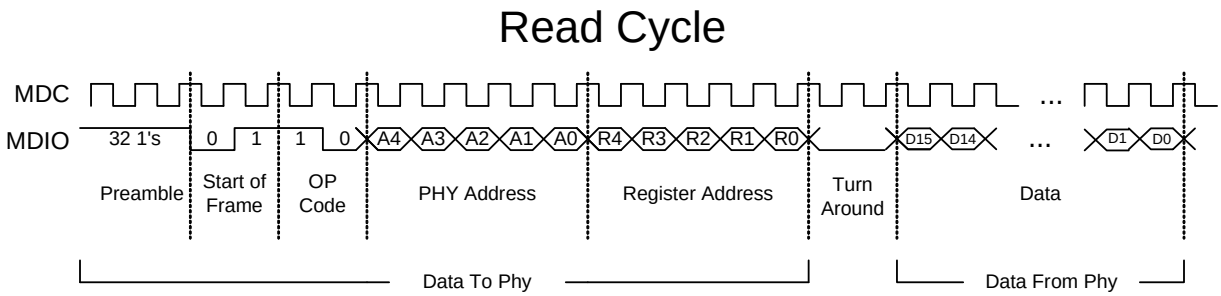
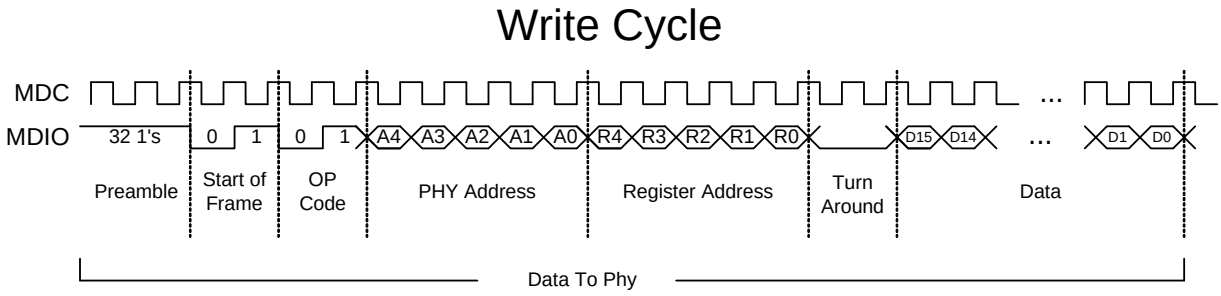


FIGURE 3-6: MDIO TIMING AND FRAME STRUCTURE - WRITE CYCLE



3.6 Interrupt Management

The device management interface supports an interrupt capability that is not a part of the IEEE 802.3 specification. This interrupt capability generates an active low asynchronous interrupt signal on the nINT output whenever certain events are detected as setup by the Interrupt Mask Register.

The device’s interrupt system provides two modes, a Primary Interrupt mode and an Alternative interrupt mode. Both systems will assert the nINT pin low when the corresponding mask bit is set. These modes differ only in how they de-assert the nINT interrupt output. These modes are detailed in the following subsections.

Note: The Primary interrupt mode is the default interrupt mode after a power-up or hard reset. The Alternative interrupt mode requires setup after a power-up or hard reset.

3.6.1 PRIMARY INTERRUPT SYSTEM

The Primary interrupt system is the default interrupt mode (ALTINT bit of the Mode Control/Status Register is “0”). The Primary interrupt system is always selected after power-up or hard reset. In this mode, to set an interrupt, set the corresponding mask bit in the Interrupt Mask Register (see Table 3-3). Then when the event to assert nINT is true, the nINT output will be asserted. When the corresponding event to deassert nINT is true, then the nINT will be de-asserted.

TABLE 3-3: INTERRUPT MANAGEMENT TABLE

Mask	Interrupt Source Flag		Interrupt Source		Event to Assert nINT	Event to De-Assert nINT
30.7	29.7	ENERGYON	17.1	ENERGYON	Rising 17.1 (Note 3-3)	Falling 17.1 or Reading register 29
30.6	29.6	Auto-Negotiation complete	1.5	Auto-Negotiate Complete	Rising 1.5	Falling 1.5 or Reading register 29
30.5	29.5	Remote Fault Detected	1.4	Remote Fault	Rising 1.4	Falling 1.4, or Reading register 1 or Reading register 29
30.4	29.4	Link Down	1.2	Link Status	Falling 1.2	Reading register 1 or Reading register 29
30.3	29.3	Auto-Negotiation LP Acknowledge	5.14	Acknowledge	Rising 5.14	Falling 5.14 or Read register 29
30.2	29.2	Parallel Detection Fault	6.4	Parallel Detection Fault	Rising 6.4	Falling 6.4 or Reading register 6, or Reading register 29 or Re-Auto Negotiate or Link down
30.1	29.1	Auto-Negotiation Page Received	6.1	Page Received	Rising 6.1	Falling of 6.1 or Reading register 6, or Reading register 29 Re-Auto Negotiate, or Link Down.

Note 3-3 If the mask bit is enabled and nINT has been de-asserted while ENERGYON is still high, nINT will assert for 256 ms, approximately one second after ENERGYON goes low when the Cable is unplugged. To prevent an unexpected assertion of nINT, the ENERGYON interrupt mask should always be cleared as part of the ENERGYON interrupt service routine.

Note: The ENERGYON bit in the Mode Control/Status Register is defaulted to a ‘1’ at the start of the signal acquisition process, therefore the INT7 bit in the Interrupt Mask Register will also read as a ‘1’ at power-up. If no signal is present, then both ENERGYON and INT7 will clear within a few milliseconds.

3.6.2 ALTERNATE INTERRUPT SYSTEM

The Alternate interrupt system is enabled by setting the ALTINT bit of the Mode Control/Status Register to “1”. In this mode, to set an interrupt, set the corresponding bit of the in the Mask Register 30, (see Table 3-4). To Clear an interrupt, either clear the corresponding bit in the Interrupt Mask Register to deassert the nINT output, or clear the interrupt source, and write a ‘1’ to the corresponding Interrupt Source Flag. Writing a ‘1’ to the Interrupt Source Flag will cause the state machine to check the Interrupt Source to determine if the Interrupt Source Flag should clear or stay as a ‘1’. If the Condition to deassert is true, then the Interrupt Source Flag is cleared and nINT is also deasserted. If the Condition to deassert is false, then the Interrupt Source Flag remains set, and the nINT remains asserted.

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For example, setting the INT7 bit in the Interrupt Mask Register will enable the ENERGYON interrupt. After a cable is plugged in, the ENERGYON bit in the Mode Control/Status Register goes active and nINT will be asserted low. To de-assert the nINT interrupt output, either clear the ENERGYON bit in the Mode Control/Status Register by removing the cable and then writing a '1' to the INT7 bit in the Interrupt Mask Register, *OR* clear the INT7 mask (bit 7 of the Interrupt Mask Register).

TABLE 3-4: ALTERNATIVE INTERRUPT SYSTEM MANAGEMENT TABLE

Mask	Interrupt Source Flag		Interrupt Source		Event to Assert nINT	Condition to De-Assert	Bit to Clear nINT
30.7	29.7	ENERGYON	17.1	ENERGYON	Rising 17.1	17.1 low	29.7
30.6	29.6	Auto-Negotiation complete	1.5	Auto-Negotiate Complete	Rising 1.5	1.5 low	29.6
30.5	29.5	Remote Fault Detected	1.4	Remote Fault	Rising 1.4	1.4 low	29.5
30.4	29.4	Link Down	1.2	Link Status	Falling 1.2	1.2 high	29.4
30.3	29.3	Auto-Negotiation LP Acknowledge	5.14	Acknowledge	Rising 5.14	5.14 low	29.3
30.2	29.2	Parallel Detection Fault	6.4	Parallel Detection Fault	Rising 6.4	6.4 low	29.2
30.1	29.1	Auto-Negotiation Page Received	6.1	Page Received	Rising 6.1	6.1 low	29.1

Note: The ENERGYON bit in the Mode Control/Status Register is defaulted to a '1' at the start of the signal acquisition process, therefore the INT7 bit in the Interrupt Mask Register will also read as a '1' at power-up. If no signal is present, then both ENERGYON and INT7 will clear within a few milliseconds.

3.7 Configuration Straps

Configuration straps allow various features of the device to be automatically configured to user defined values. Configuration straps are latched upon Power-On Reset (POR) and pin reset (nRST). Configuration straps include internal resistors in order to prevent the signal from floating when unconnected. If a particular configuration strap is connected to a load, an external pull-up or pull-down resistor should be used to augment the internal resistor to ensure that it reaches the required voltage level prior to latching. The internal resistor can also be overridden by the addition of an external resistor.

Note 3-4 The system designer must guarantee that configuration strap pins meet the timing requirements specified in Section 5.5.3, "Power-On nRST & Configuration Strap Timing," on page 59. If configuration strap pins are not at the correct voltage level prior to being latched, the device may capture incorrect strap values.

Note 3-5 When externally pulling configuration straps high, the strap should be tied to VDDIO, except for REGOFF and nINTSEL which should be tied to VDD2A.

3.7.1 PHYAD[2:0]: PHY ADDRESS CONFIGURATION

The PHYAD[2:0] configuration straps are driven high or low to give each PHY a unique address. This address is latched into an internal register at the end of a hardware reset (default = 000b). In a multi-transceiver application (such as a repeater), the controller is able to manage each transceiver via the unique address. Each transceiver checks each management data frame for a matching address in the relevant bits. When a match is recognized, the transceiver responds to that particular frame. The PHY address is also used to seed the scrambler. In a multi-transceiver application, this ensures that the scramblers are out of synchronization and disperses the electromagnetic radiation across the frequency spectrum.

The device's SMI address may be configured using hardware configuration to any value between 0 and 7. The user can configure the PHY address using Software Configuration if an address greater than 7 is required. The PHY address can be written (after SMI communication at some address is established) using the PHYAD bits of the Special Modes Register. The PHYAD[2:0] configuration straps are multiplexed with other signals as shown in Table 3-5.

TABLE 3-5: PIN NAMES FOR ADDRESS BITS

Address Bit	Pin Name
PHYAD[0]	RXER/RXD4/PHYAD0
PHYAD[1]	RXCLK/PHYAD1
PHYAD[2]	RXD3/PHYAD2

3.7.2 MODE[2:0]: MODE CONFIGURATION

The MODE[2:0] configuration straps control the configuration of the 10/100 digital block. When the nRST pin is deasserted, the register bit values are loaded according to the MODE[2:0] configuration straps. The 10/100 digital block is then configured by the register bit values. When a soft reset occurs via the Soft Reset bit of the Basic Control Register, the configuration of the 10/100 digital block is controlled by the register bit values and the MODE[2:0] configuration straps have no affect.

The device's mode may be configured using the hardware configuration straps as summarized in Table 3-6. The user may configure the transceiver mode by writing the SMI registers.

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TABLE 3-6: MODE[2:0] BUS

MODE[2:0]	Mode Definitions	Default Register Bit Values	
		Register 0	Register 4
		[13,12,10,8]	[8,7,6,5]
000	10Base-T Half Duplex. Auto-negotiation disabled.	0000	N/A
001	10Base-T Full Duplex. Auto-negotiation disabled.	0001	N/A
010	100Base-TX Half Duplex. Auto-negotiation disabled. CRS is active during Transmit & Receive.	1000	N/A
011	100Base-TX Full Duplex. Auto-negotiation disabled. CRS is active during Receive.	1001	N/A
100	100Base-TX Half Duplex is advertised. Auto-negotiation enabled. CRS is active during Transmit & Receive.	1100	0100
101	Repeater mode. Auto-negotiation enabled. 100Base-TX Half Duplex is advertised. CRS is active during Receive.	1100	0100
110	Power Down mode. In this mode the transceiver will wake-up in Power-Down mode. The transceiver cannot be used when the MODE[2:0] bits are set to this mode. To exit this mode, the MODE bits in Register 18.7:5(see Section 4.2.9, "Special Modes Register," on page 50) must be configured to some other value and a soft reset must be issued.	N/A	N/A
111	All capable. Auto-negotiation enabled.	X10X	1111

The MODE[2:0] hardware configuration pins are multiplexed with other signals as shown in Table 3-7.

TABLE 3-7: PIN NAMES FOR MODE BITS

MODE Bit	Pin Name
MODE[0]	RXD0/MODE0
MODE[1]	RXD1/MODE1
MODE[2]	COL/CRS_DV/MODE2

3.7.3 RMIISEL: MII/RMII MODE CONFIGURATION

MII or RMII mode selection is latched on the rising edge of the internal reset (nRST) based on the strapping of the RMIISEL configuration strap. The default mode is MII (via the internal pull-down resistor). To select RMII mode, pull the RMIISEL configuration strap high with an external resistor to VDDIO.

When the nRST pin is deasserted, the MIIMODE bit of the Special Modes Register is loaded according to the RMIISEL configuration strap. The mode is reflected in the MIIMODE bit of the Special Modes Register.

Refer to Section 3.4, "MAC Interface," on page 24 for additional information on MII and RMII modes.

3.7.4 REGOFF: INTERNAL +1.2V REGULATOR CONFIGURATION

The incorporation of flexPWR technology provides the ability to disable the internal +1.2V regulator. When the regulator is disabled, an external +1.2V must be supplied to the VDDCR pin. Disabling the internal +1.2V regulator makes it possible to reduce total system power, since an external switching regulator with greater efficiency (versus the internal linear regulator) can be used to provide +1.2V to the transceiver circuitry.

Note: Because the REGOFF configuration strap shares functionality with the LED1 pin, proper consideration must also be given to the LED polarity. Refer to Section 3.8.1.1, "REGOFF and LED1 Polarity Selection," on page 33 for additional information on the relation between REGOFF and the LED1 polarity.

3.7.4.1 Disabling the Internal +1.2V Regulator

To disable the +1.2V internal regulator, a pull-up strapping resistor should be connected from the REGOFF configuration strap to VDD2A. At power-on, after both VDDIO and VDD2A are within specification, the transceiver will sample REGOFF to determine whether the internal regulator should turn on. If the pin is sampled at a voltage greater than V_{IH}, then the internal regulator is disabled and the system must supply +1.2V to the VDDCR pin. The VDDIO voltage must be at least 80% of the operating voltage level (1.44V when operating at 1.8V, 2.0V when operating at 2.5V, 2.64V when operating at 3.3V) before voltage is applied to VDDCR. As described in Section 3.7.4.2, when REGOFF is left floating or connected to VSS, the internal regulator is enabled and the system is not required to supply +1.2V to the VDDCR pin.

3.7.4.2 Enabling the Internal +1.2V Regulator

The +1.2V for VDDCR is supplied by the on-chip regulator unless the transceiver is configured for the regulator off mode using the REGOFF configuration strap as described in Section 3.7.4.1. By default, the internal +1.2V regulator is enabled when REGOFF is floating (due to the internal pull-down resistor). During power-on, if REGOFF is sampled below V_{IL}, then the internal +1.2V regulator will turn on and operate with power from the VDD2A pin.

3.7.5 NINTSEL: NINT/TXER/TXD4 CONFIGURATION

The nINT, TXER, and TXD4 functions share a common pin. There are two functional modes for this pin, the TXER/TXD4 mode and nINT (interrupt) mode. The nINTSEL configuration strap is latched at POR and on the rising edge of the nRST. By default, nINTSEL is configured for nINT mode via the internal pull-up resistor.

Note: Because the nINTSEL configuration strap shares functionality with the LED2 pin, proper consideration must also be given to the LED polarity. Refer to Section 3.8.1.2, "nINTSEL and LED2 Polarity Selection," on page 33 for additional information on the relation between nINTSEL and the LED2 polarity.

3.8 Miscellaneous Functions

3.8.1 LEDS

Two LED signals are provided as a convenient means to determine the transceiver's mode of operation. All LED signals are either active high or active low as described in Section 3.8.1.2, "nINTSEL and LED2 Polarity Selection" and Section 3.8.1.1, "REGOFF and LED1 Polarity Selection," on page 33.

The LED1 output is driven active whenever the device detects a valid link, and blinks when CRS is active (high) indicating activity.

The LED2 output is driven active when the operating speed is 100Mbps. This LED will go inactive when the operating speed is 10Mbps or during line isolation.

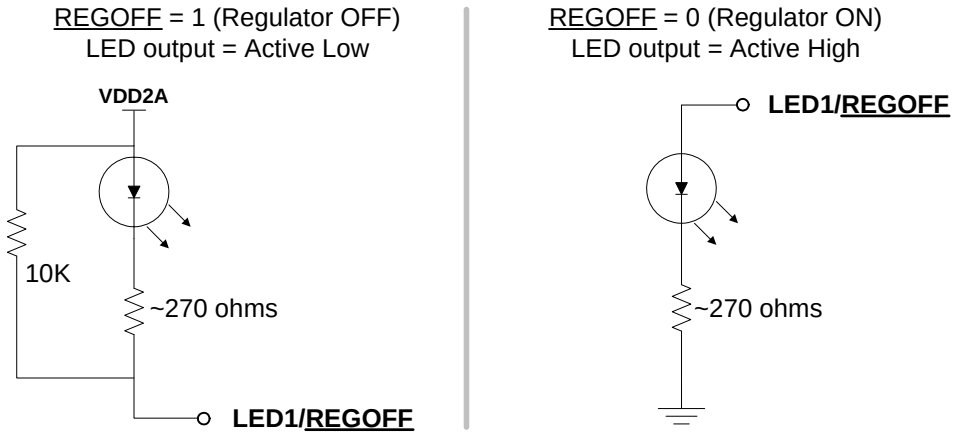
Note: When pulling the LED1 and LED2 pins high, they must be tied to VDD2A, **NOT** VDDIO.

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3.8.1.1 REGOFF and LED1 Polarity Selection

The REGOFF configuration strap is shared with the LED1 pin. The LED1 output will automatically change polarity based on the presence of an external pull-up resistor. If the LED1 pin is pulled high to VDD2A by an external pull-up resistor to select a logical high for REGOFF, then the LED1 output will be active low. If the LED1 pin is pulled low by the internal pull-down resistor to select a logical low for REGOFF, the LED1 output will then be an active high output. Figure 3-7 details the LED1 polarity for each REGOFF configuration.

FIGURE 3-7: LED1/REGOFF POLARITY CONFIGURATION

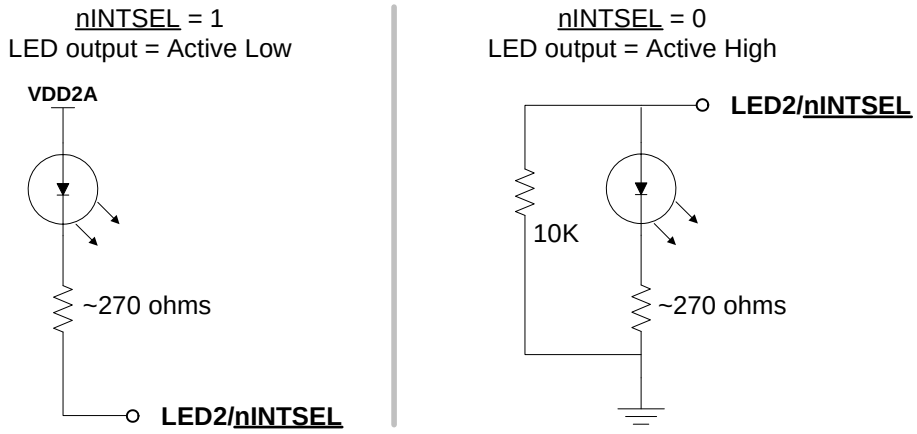


Note: Refer to Section 3.7.4, "REGOFF: Internal +1.2V Regulator Configuration," on page 32 for additional information on the REGOFF configuration strap.

3.8.1.2 nINTSEL and LED2 Polarity Selection

The nINTSEL configuration strap is shared with the LED2 pin. The LED2 output will automatically change polarity based on the presence of an external pull-down resistor. If the LED2 pin is pulled high to VDD2A to select a logical high for nINTSEL, then the LED2 output will be active low. If the LED2 pin is pulled low by an external pull-down resistor to select a logical low for nINTSEL, the LED2 output will then be an active high output. Figure 3-8 details the LED2 polarity for each nINTSEL configuration.

FIGURE 3-8: LED2/NINTSEL POLARITY CONFIGURATION



Note: Refer to Section 3.7.5, "nINTSEL: nINT/TXER/TXD4 Configuration," on page 32 for additional information on the nINTSEL configuration strap.

3.8.2 VARIABLE VOLTAGE I/O

The device's digital I/O pins are variable voltage, allowing them to take advantage of low power savings from shrinking technologies. These pins can operate from a low I/O voltage of +1.62V up to +3.6V. The applied I/O voltage must maintain its value with a tolerance of ± 10%. Varying the voltage up or down after the transceiver has completed power-on reset can cause errors in the transceiver operation. Refer to Section 5.0, "Operational Characteristics," on page 54 for additional information.

Note: Input signals must not be driven high before power is applied to the device.

3.8.3 POWER-DOWN MODES

There are two device power-down modes: General Power-Down Mode and Energy Detect Power-Down Mode. These modes are described in the following subsections.

3.8.3.1 General Power-Down

This power-down mode is controlled via the Power Down bit of the Basic Control Register. In this mode, the entire transceiver (except the management interface) is powered-down and remains in this mode as long as the Power Down bit is "1". When the Power Down bit is cleared, the transceiver powers up and is automatically reset.

3.8.3.2 Energy Detect Power-Down

This power-down mode is activated by setting the EDPWRDOWN bit of the Mode Control/Status Register. In this mode, when no energy is present on the line the transceiver is powered down (except for the management interface, the SQUELCH circuit, and the ENERGYON logic). The ENERGYON logic is used to detect the presence of valid energy from 100BASE-TX, 10BASE-T, or Auto-negotiation signals.

In this mode, when the ENERGYON bit of the Mode Control/Status Register is low, the transceiver is powered-down and nothing is transmitted. When energy is received via link pulses or packets, the ENERGYON bit goes high and the transceiver powers-up. The device automatically resets into the state prior to power-down and asserts the nINT interrupt if the ENERGYON interrupt is enabled in the Interrupt Mask Register. The first and possibly the second packet to activate ENERGYON may be lost.

When the EDPWRDOWN bit of the Mode Control/Status Register is low, energy detect power-down is disabled.

3.8.4 ISOLATE MODE

The device data paths may be electrically isolated from the MII/RMII interface by setting the Isolate bit of the Basic Control Register to "1". In isolation mode, the transceiver does not respond to the TXD, TXEN and TXER inputs, but does respond to management transactions.

Isolation provides a means for multiple transceivers to be connected to the same MII/RMII interface without contention. By default, the transceiver is not isolated (on power-up (Isolate=0).

3.8.5 RESETS

The device provides two forms of reset: Hardware and Software. The device registers are reset by both Hardware and Software resets. Select register bits, indicated as "NASR" in the register definitions, are not cleared by a Software reset. The registers are not reset by the power-down modes described in Section 3.8.3.

Note: For the first 16us after coming out of reset, the MII/RMII interface will run at 2.5 MHz. After this time, it will switch to 25 MHz if auto-negotiation is enabled.

3.8.5.1 Hardware Reset

A Hardware reset is asserted by driving the nRST input pin low. When driven, nRST should be held low for the minimum time detailed in Section 5.5.3, "Power-On nRST & Configuration Strap Timing," on page 59 to ensure a proper transceiver reset. During a Hardware reset, an external clock ***must*** be supplied to the XTAL1/CLKIN signal.

Note: A hardware reset (nRST assertion) is required following power-up. Refer to Section 5.5.3, "Power-On nRST & Configuration Strap Timing," on page 59 for additional information.

3.8.5.2 Software Reset

A Software reset is activated by setting the Soft Reset bit of the Basic Control Register to "1". All registers bits, except those indicated as "NASR" in the register definitions, are cleared by a Software reset. The Soft Reset bit is self-clearing. Per the IEEE 802.3u standard, clause 22 (22.2.4.1.1) the reset process will be completed within 0.5s from the setting of this bit.

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3.8.6 CARRIER SENSE

The carrier sense (CRS) is output on the CRS pin in MII mode, and the CRS_DV pin in RMII mode. CRS is a signal defined by the MII specification in the IEEE 802.3u standard. The device asserts CRS based only on receive activity whenever the transceiver is either in repeater mode or full-duplex mode. Otherwise the transceiver asserts CRS based on either transmit or receive activity.

The carrier sense logic uses the encoded, unscrambled data to determine carrier activity status. It activates carrier sense with the detection of 2 non-contiguous zeros within any 10 bit span. Carrier sense terminates if a span of 10 consecutive ones is detected before a /J/K/ Start-of Stream Delimiter pair. If an SSD pair is detected, carrier sense is asserted until either /T/R/ End–of-Stream Delimiter pair or a pair of IDLE symbols is detected. Carrier is negated after the /T/ symbol or the first IDLE. If /T/ is not followed by /R/, then carrier is maintained. Carrier is treated similarly for IDLE followed by some non-IDLE symbol.

3.8.7 COLLISION DETECT

A collision is the occurrence of simultaneous transmit and receive operations. The COL output is asserted to indicate that a collision has been detected. COL remains active for the duration of the collision. COL is changed asynchronously to both RXCLK and TXCLK. The COL output becomes inactive during full duplex mode.

The COL may be tested by setting the Collision Test bit of the Basic Control Register to “1”. This enables the collision test. COL will be asserted within 512 bit times of TXEN rising and will be de-asserted within 4 bit times of TXEN falling.

3.8.8 LINK INTEGRITY TEST

The device performs the link integrity test as outlined in the IEEE 802.3u (Clause 24-15) Link Monitor state diagram. The link status is multiplexed with the 10Mbps link status to form the Link Status bit in the Basic Status Register and to drive the LINK LED (LED1).

The DSP indicates a valid MLT-3 waveform present on the RXP and RXN signals as defined by the ANSI X3.263 TP-PMD standard, to the Link Monitor state-machine, using the internal DATA_VALID signal. When DATA_VALID is asserted, the control logic moves into a Link-Ready state and waits for an enable from the auto-negotiation block. When received, the Link-Up state is entered, and the Transmit and Receive logic blocks become active. Should auto-negotiation be disabled, the link integrity logic moves immediately to the Link-Up state when the DATA_VALID is asserted.

To allow the line to stabilize, the link integrity logic will wait a minimum of 330 μsec from the time DATA_VALID is asserted until the Link-Ready state is entered. Should the DATA_VALID input be negated at any time, this logic will immediately negate the Link signal and enter the Link-Down state.

When the 10/100 digital block is in 10BASE-T mode, the link status is derived from the 10BASE-T receiver logic.

3.8.9 LOOPBACK OPERATION

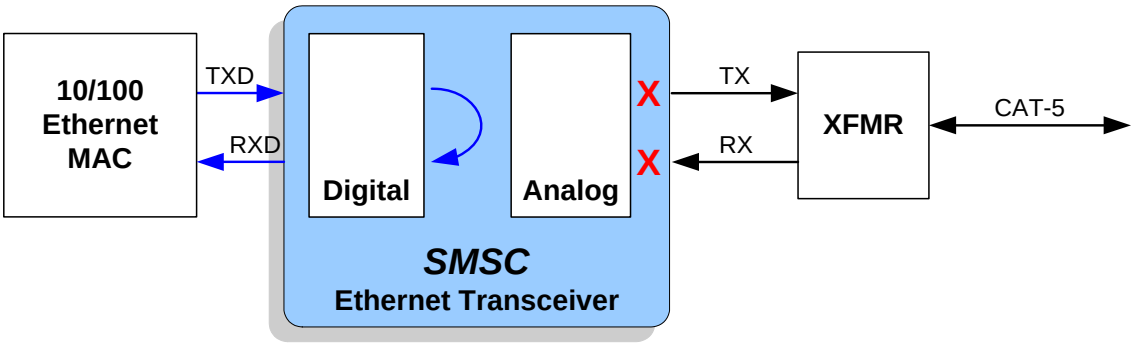
The device may be configured for near-end loopback and far loopback. These loopback modes are detailed in the following subsections.

3.8.9.1 Near-end Loopback

Near-end loopback mode sends the digital transmit data back out the receive data signals for testing purposes, as indicated by the blue arrows in Figure 3-9. The near-end loopback mode is enabled by setting the Loopback bit of the Basic Control Register to “1”. A large percentage of the digital circuitry is operational in near-end loopback mode because data

is routed through the PCS and PMA layers into the PMD sublayer before it is looped back. The COL signal will be inactive in this mode, unless Collision Test is enabled in the Basic Control Register. The transmitters are powered down regardless of the state of TXEN.

FIGURE 3-9: NEAR-END LOOPBACK BLOCK DIAGRAM

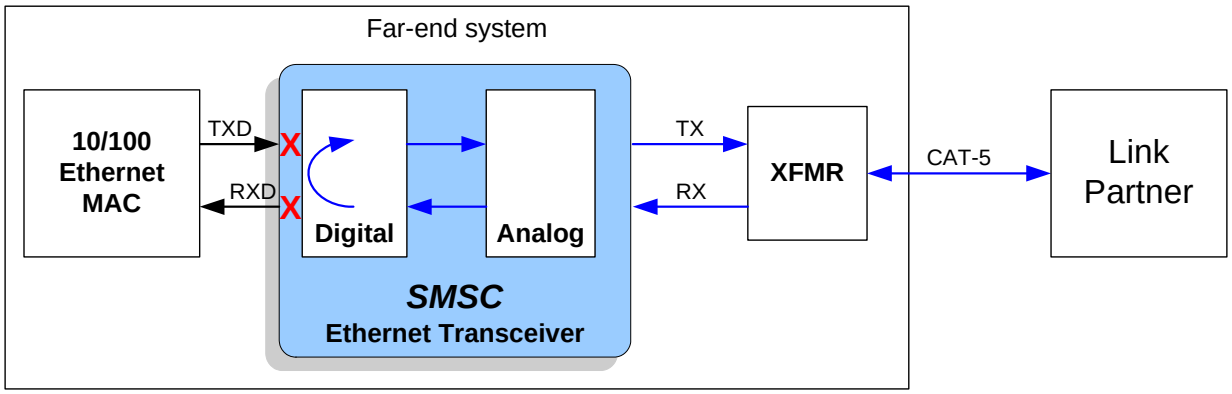


3.8.9.2 Far Loopback

Far loopback is a special test mode for MDI (analog) loopback as indicated by the blue arrows in Figure 3-11. The far loopback mode is enabled by setting the FARLOOPBACK bit of the Mode Control/Status Register to “1”. In this mode, data that is received from the link partner on the MDI is looped back out to the link partner. The digital interface signals on the local MAC interface are isolated.

Note: This special test mode is only available when operating in RMII mode.

FIGURE 3-10: FAR LOOPBACK BLOCK DIAGRAM

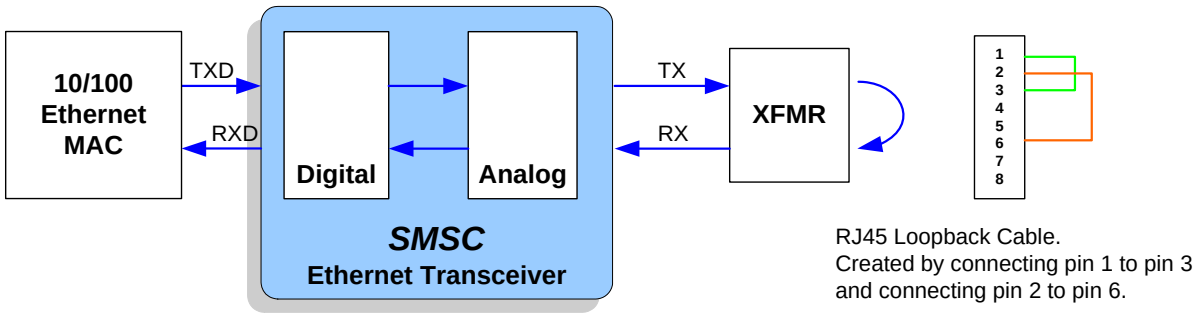


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3.8.9.3 Connector Loopback

The device maintains reliable transmission over very short cables, and can be tested in a connector loopback as shown in Figure 3-11. An RJ45 loopback cable can be used to route the transmit signals an the output of the transformer back to the receiver inputs, and this loopback will work at both 10 and 100.

FIGURE 3-11: CONNECTOR LOOPBACK BLOCK DIAGRAM



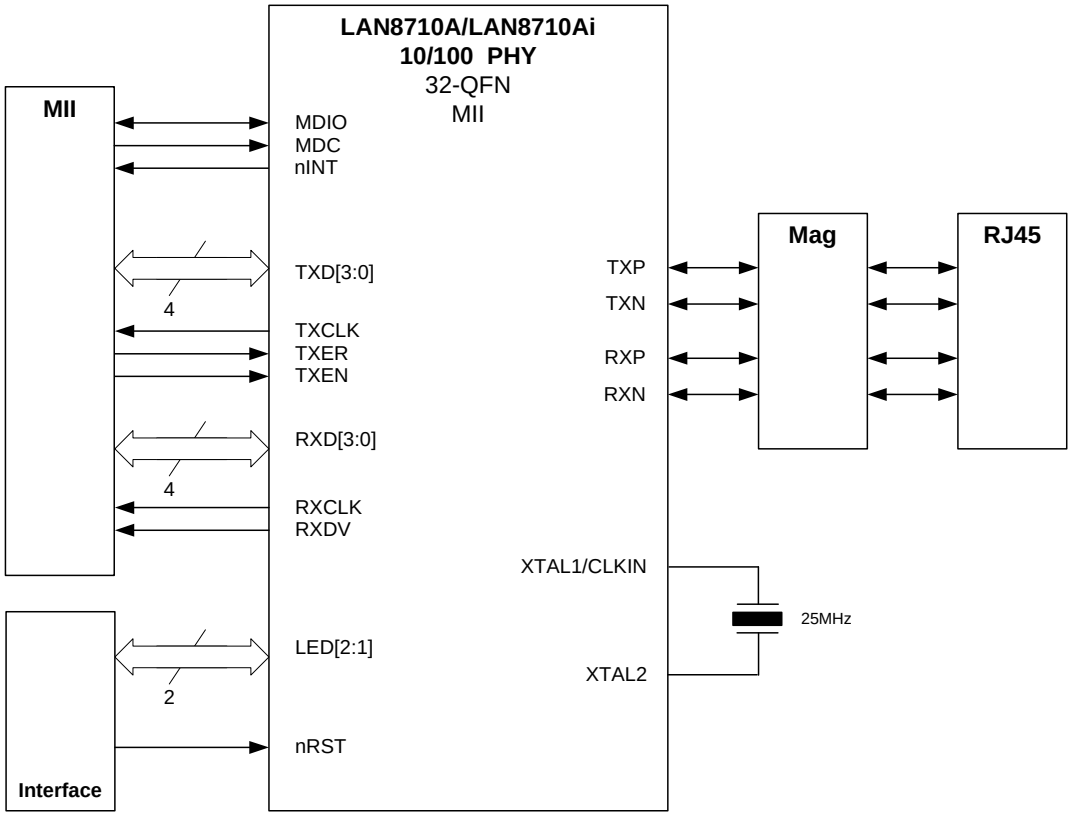
3.9 Application Diagrams

This section provides typical application diagrams for the following:

- Simplified System Level Application Diagram
- Power Supply Diagram (1.2V Supplied by Internal Regulator)
- Power Supply Diagram (1.2V Supplied by External Source)
- Twisted-Pair Interface Diagram (Single Power Supply)
- Twisted-Pair Interface Diagram (Dual Power Supplies)

3.9.1 SIMPLIFIED SYSTEM LEVEL APPLICATION DIAGRAM

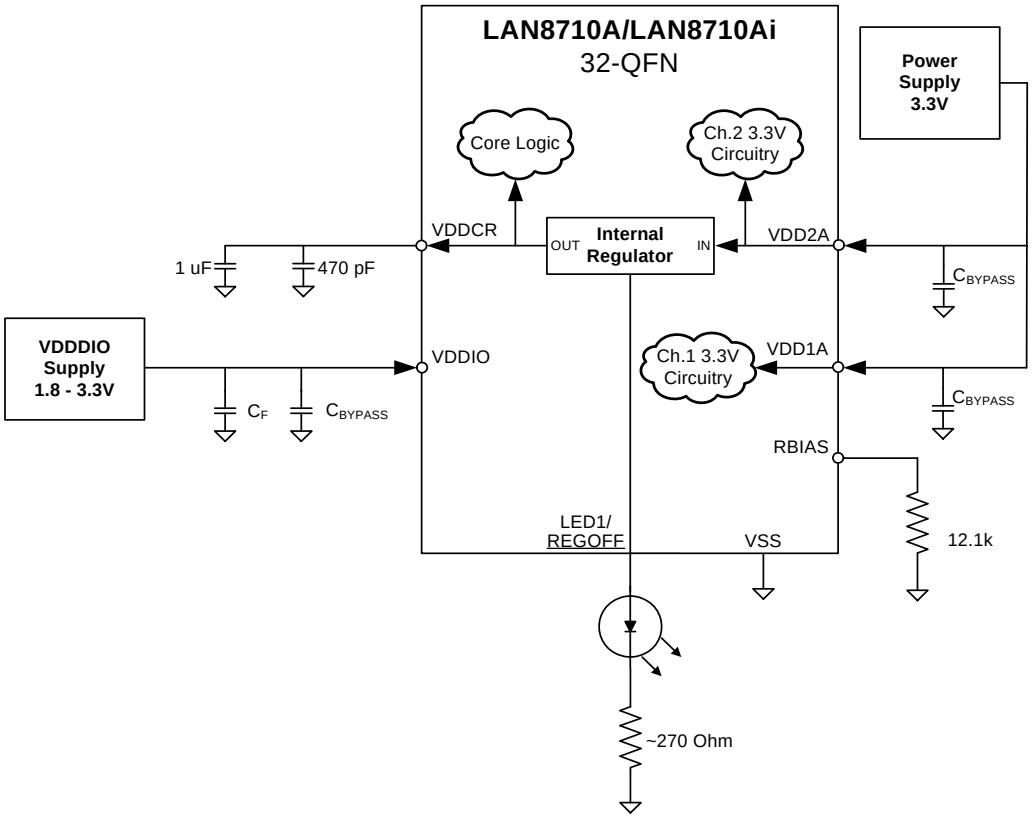
FIGURE 3-12: SIMPLIFIED SYSTEM LEVEL APPLICATION DIAGRAM



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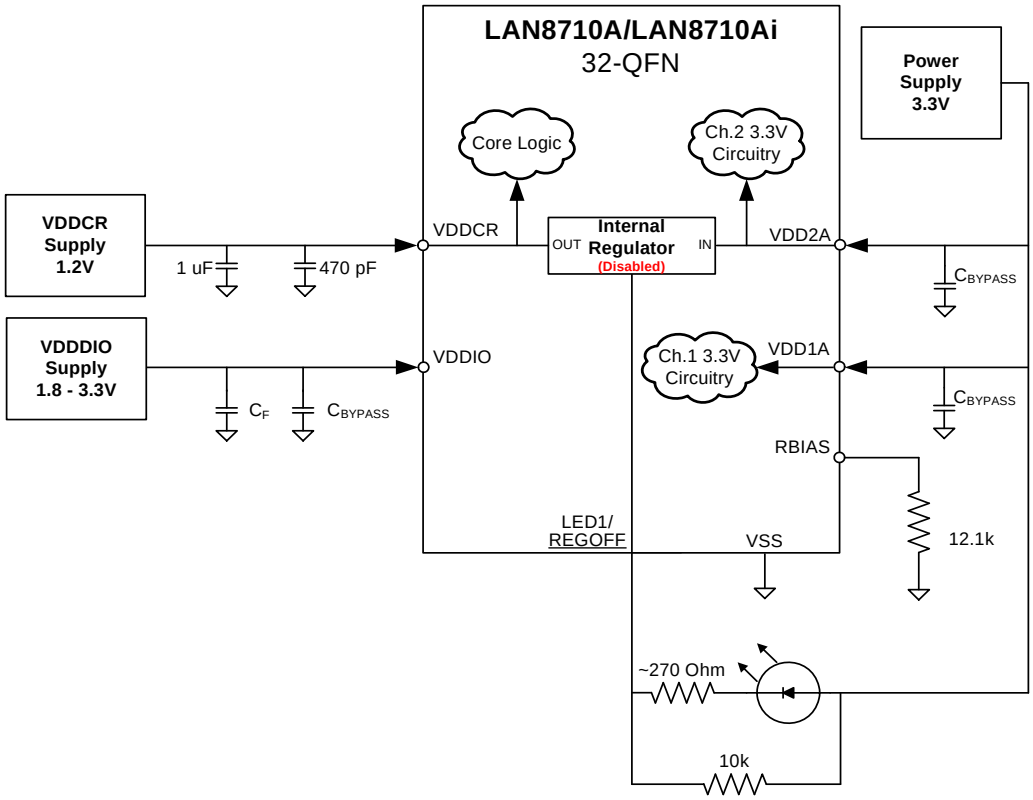
3.9.2 POWER SUPPLY DIAGRAM (1.2V SUPPLIED BY INTERNAL REGULATOR)

FIGURE 3-13: POWER SUPPLY DIAGRAM (1.2V SUPPLIED BY INTERNAL REGULATOR)



3.9.3 POWER SUPPLY DIAGRAM (1.2V SUPPLIED BY EXTERNAL SOURCE)

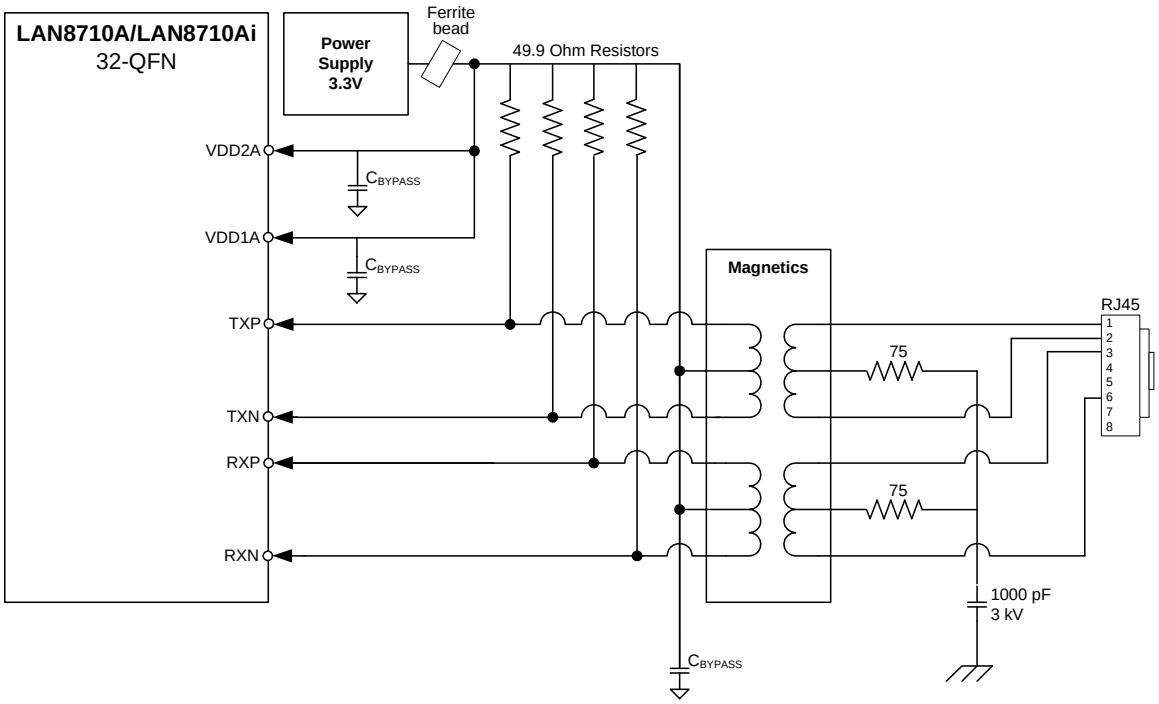
FIGURE 3-14: POWER SUPPLY DIAGRAM (1.2V SUPPLIED BY EXTERNAL SOURCE)



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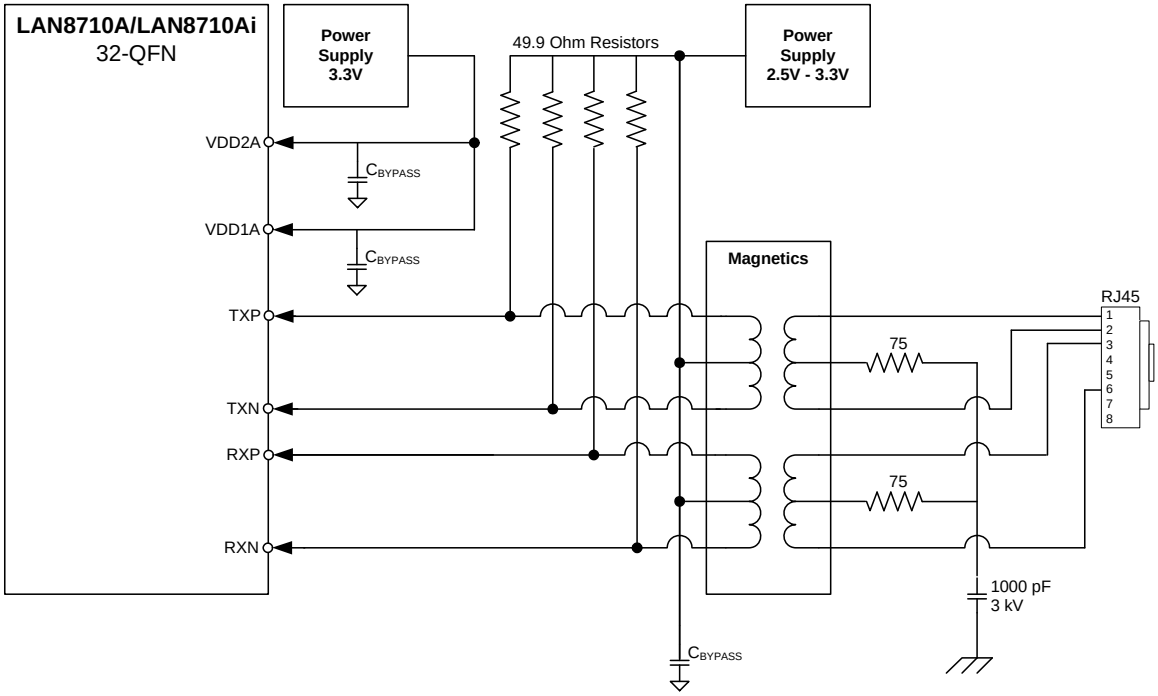
3.9.4 TWISTED-PAIR INTERFACE DIAGRAM (SINGLE POWER SUPPLY)

FIGURE 3-15: TWISTED-PAIR INTERFACE DIAGRAM (SINGLE POWER SUPPLY)



3.9.5 TWISTED-PAIR INTERFACE DIAGRAM (DUAL POWER SUPPLIES)

FIGURE 3-16: TWISTED-PAIR INTERFACE DIAGRAM (DUAL POWER SUPPLIES)



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4.0 REGISTER DESCRIPTIONS

This chapter describes the various control and status registers (CSRs). All registers follow the IEEE 802.3 (clause 22.2.4) management register set. All functionality and bit definitions comply with these standards. The IEEE 802.3 specified register index (in decimal) is included with each register definition, allowing for addressing of these registers via the Serial Management Interface (SMI) protocol.

4.1 Register Nomenclature

Table 4-1 describes the register bit attribute notation used throughout this document.

TABLE 4-1: REGISTER BIT TYPES

Register Bit Type Notation	Register Bit Description
R	**Read:** A register or bit with this attribute can be read.
W	**Read:** A register or bit with this attribute can be written.
RO	**Read only:** Read only. Writes have no effect.
WO	**Write only:** If a register or bit is write-only, reads will return unspecified data.
WC	**Write One to Clear:** writing a one clears the value. Writing a zero has no effect
WAC	**Write Anything to Clear:** writing anything clears the value.
RC	**Read to Clear:** Contents is cleared after the read. Writes have no effect.
LL	**Latch Low:** Clear on read of register.
LH	**Latch High:** Clear on read of register.
SC	**Self-Clearing:** Contents are self-cleared after the being set. Writes of zero have no effect. Contents can be read.
SS	**Self-Setting:** Contents are self-setting after being cleared. Writes of one have no effect. Contents can be read.
RO/LH	**Read Only, Latch High:** Bits with this attribute will stay high until the bit is read. After it is read, the bit will either remain high if the high condition remains, or will go low if the high condition has been removed. If the bit has not been read, the bit will remain high regardless of a change to the high condition. This mode is used in some Ethernet PHY registers.
NASR	**Not Affected by Software Reset.** The state of NASR bits do not change on assertion of a software reset.
RESERVED	**Reserved Field:** Reserved fields must be written with zeros to ensure future compatibility. The value of reserved bits is not guaranteed on a read.

Many of these register bit notations can be combined. Some examples of this are shown below:

- **R/W:** Can be written. Will return current setting on a read.
- **R/WAC:** Will return current setting on a read. Writing anything clears the bit.

4.2 Control and Status Registers

Table 4-2 provides a list of supported registers. Register details, including bit definitions, are provided in the proceeding subsections.

TABLE 4-2: SMI REGISTER MAP

Register Index (Decimal)	Register Name	Group
0	Basic Control Register	Basic
1	Basic Status Register	Basic
2	PHY Identifier 1	Extended
3	PHY Identifier 2	Extended
4	Auto-Negotiation Advertisement Register	Extended
5	Auto-Negotiation Link Partner Ability Register	Extended
6	Auto-Negotiation Expansion Register	Extended
17	Mode Control/Status Register	Vendor-specific
18	Special Modes	Vendor-specific
26	Symbol Error Counter Register	Vendor-specific
27	Control / Status Indication Register	Vendor-specific
29	Interrupt Source Register	Vendor-specific
30	Interrupt Mask Register	Vendor-specific
31	PHY Special Control/Status Register	Vendor-specific

4.2.1 BASIC CONTROL REGISTER

Index (In Decimal): 0 Size: 16 bits

Bits	Description	Type	Default
15	**Soft Reset** 1 = software reset. Bit is self-clearing. When setting this bit do not set other bits in this register. The configuration (as described in Section 3.7.2, MODE[2:0]: Mode Configuration) is set from the register bit values, and not from the mode pins.	R/W SC	0b
14	**Loopback** 0 = normal operation 1 = loopback mode	R/W	0b
13	**Speed Select** 0 = 10Mbps 1 = 100Mbps Ignored if Auto-negotiation is enabled (0.12 = 1).	R/W	Note 4-1
12	**Auto-Negotiation Enable** 0 = disable auto-negotiate process 1 = enable auto-negotiate process (overrides 0.13 and 0.8)	R/W	Note 4-1

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Bits	Description	Type	Default
11	**Power Down** 0 = normal operation 1 = General power down mode The Auto-Negotiation Enable must be cleared before setting the Power Down.	R/W	0b
10	**Isolate** 0 = normal operation 1 = electrical isolation of PHY from the MII/RMII	R/W	0b
9	**Restart Auto-Negotiate** 0 = normal operation 1 = restart auto-negotiate process Bit is self-clearing.	R/W SC	0b
8	**Duplex Mode** 0 = half duplex 1 = full duplex Ignored if Auto-Negotiation is enabled (0.12 = 1).	R/W	Note 4-1
7	**Collision Test** 0 = disable COL test 1 = enable COL test	R/W	0b
6:0	**RESERVED**	RO	—

Note 4-1 The default value of this bit is determined by the MODE[2:0] configuration straps. Refer to Section 3.7.2, MODE[2:0]: Mode Configuration for additional information.

4.2.2 BASIC STATUS REGISTER

Index (In Decimal): 1 Size: 16 bits

Bits	Description	Type	Default
15	100BASE-T4 0 = no T4 ability 1 = T4 able	RO	0b
14	100BASE-TX Full Duplex 0 = no TX full duplex ability 1 = TX with full duplex	RO	1b
13	100BASE-TX Half Duplex 0 = no TX half duplex ability 1 = TX with half duplex	RO	1b
12	10BASE-T Full Duplex 0 = no 10Mbps with full duplex ability 1 = 10Mbps with full duplex	RO	1b
11	10BASE-T Half Duplex 0 = no 10Mbps with half duplex ability 1 = 10Mbps with half duplex	RO	1b

Bits	Description	Type	Default
10	100BASE-T2 Full Duplex 0 = PHY not able to perform full duplex 100BASE-T2 1 = PHY able to perform full duplex 100BASE-T2	RO	0b
9	100BASE-T2 Half Duplex 0 = PHY not able to perform half duplex 100BASE-T2 1 = PHY able to perform half duplex 100BASE-T2	RO	0b
8	Extended Status 0 = no extended status information in register 15 1 = extended status information in register 15	RO	0b
7:6	**RESERVED**	RO	—
5	Auto-Negotiate Complete 0 = auto-negotiate process not completed 1 = auto-negotiate process completed	RO	0b
4	Remote Fault 1 = remote fault condition detected 0 = no remote fault	RO/LH	0b
3	Auto-Negotiate Ability 0 = unable to perform auto-negotiation function 1 = able to perform auto-negotiation function	RO	1b
2	Link Status 0 = link is down 1 = link is up	RO/LL	0b
1	Jabber Detect 0 = no jabber condition detected 1 = jabber condition detected	RO/LH	0b
0	Extended Capabilities 0 = does not support extended capabilities registers 1 = supports extended capabilities registers	RO	1b

4.2.3 PHY IDENTIFIER 1 REGISTER

Index (In Decimal): 2 Size: 16 bits

Bits	Description	Type	Default
15:0	PHY ID Number Assigned to the 3rd through 18th bits of the Organizationally Unique Identifier (OUI), respectively.	R/W	0007h

4.2.4 PHY IDENTIFIER 2 REGISTER

Index (In Decimal): 3 Size: 16 bits

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Bits	Description	Type	Default
15:10	PHY ID Number Assigned to the 19th through 24th bits of the OUI.	R/W	110000b
9:4	Model Number Six-bit manufacturer's model number.	R/W	001111b
3:0	Revision Number Four-bit manufacturer's revision number.	R/W	Note 4-2

Note 4-2 The default value of this field will vary dependent on the silicon revision number.

4.2.5 AUTO NEGOTIATION ADVERTISEMENT REGISTER

Index (In Decimal): 4 Size: 16 bits

Bits	Description	Type	Default
15:14	**RESERVED**	RO	—
13	Remote Fault 0 = no remote fault 1 = remote fault detected	R/W	0b
12	**RESERVED**	RO	—
11:10	**Pause Operation** 00 = No PAUSE 01 = Symmetric PAUSE 10 = Asymmetric PAUSE toward link partner 11 = Advertise support for both Symmetric PAUSE and Asymmetric PAUSE toward local device **Note:** When both Symmetric PAUSE and Asymmetric PAUSE are set, the device will only be configured to, at most, one of the two settings upon auto-negotiation completion.	R/W	00b
9	**RESERVED**	RO	—
8	100BASE-TX Full Duplex 0 = no TX full duplex ability 1 = TX with full duplex	R/W	Note 4-3
7	100BASE-TX 0 = no TX ability 1 = TX able	R/W	1b
6	10BASE-T Full Duplex 0 = no 10Mbps with full duplex ability 1 = 10Mbps with full duplex	R/W	Note 4-3
5	10BASE-T 0 = no 10Mbps ability 1 = 10Mbps able	R/W	Note 4-3

Bits	Description	Type	Default
4:0	Selector Field 00001 = IEEE 802.3	R/W	00001b

Note 4-3 The default value of this bit is determined by the MODE[2:0] configuration straps. Refer to Section 3.7.2, MODE[2:0]: Mode Configuration for additional information.

4.2.6 AUTO NEGOTIATION LINK PARTNER ABILITY REGISTER

Index (In Decimal): 5 Size: 16 bits

Bits	Description	Type	Default
15	Next Page 0 = no next page ability 1 = next page capable **Note:** This device does not support next page ability.	RO	0b
14	Acknowledge 0 = link code word not yet received 1 = link code word received from partner	RO	0b
13	Remote Fault 0 = no remote fault 1 = remote fault detected	RO	0b
12:11	**RESERVED**	RO	—
10	Pause Operation 0 = No PAUSE supported by partner station 1 = PAUSE supported by partner station	RO	0b
9	100BASE-T4 0 = no T4 ability 1 = T4 able **Note:** This device does not support T4 ability.	RO	0b
8	100BASE-TX Full Duplex 0 = no TX full duplex ability 1 = TX with full duplex	RO	0b
7	100BASE-TX 0 = no TX ability 1 = TX able	RO	0b
6	**10BASE-T Full Duplex** 0 = no 10Mbps with full duplex ability 1 = 10Mbps with full duplex	RO	0b
5	10BASE-T 0 = no 10Mbps ability 1 = 10Mbps able	RO	0b
4:0	Selector Field 00001 = IEEE 802.3	RO	00001b

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4.2.7 AUTO NEGOTIATION EXPANSION REGISTER

Index (In Decimal): 6 Size: 16 bits

Bits	Description	Type	Default
15:5	**RESERVED**	RO	—
4	**Parallel Detection Fault** 0 = no fault detected by parallel detection logic 1 = fault detected by parallel detection logic	RO/LH	0b
3	**Link Partner Next Page Able** 0 = link partner does not have next page ability 1 = link partner has next page ability	RO	0b
2	Next Page Able 0 = local device does not have next page ability 1 = local device has next page ability	RO	0b
1	Page Received 0 = new page not yet received 1 = new page received	RO/LH	0b
0	**Link Partner Auto-Negotiation Able** 0 = link partner does not have auto-negotiation ability 1 = link partner has auto-negotiation ability	RO	0b

4.2.8 MODE CONTROL/STATUS REGISTER

Index (In Decimal): 17 Size: 16 bits

Bits	Description	Type	Default
15:14	**RESERVED**	RO	—
13	**EDPWRDOWN** Enable the Energy Detect Power-Down mode: 0 = Energy Detect Power-Down is disabled 1 = Energy Detect Power-Down is enabled	R/W	0b
12:10	RESERVED	RO	—
9	**FARLOOPBACK** Enables far loopback mode (for example, all the received packets are sent back simultaneously (in 100BASE-TX only)). This bit is only active in RMII mode. This mode works even if the Isolate bit (0.10) is set. 0 = Far loopback mode is disabled 1 = Far loopback mode is enabled Refer to Section 3.8.9.2, Far Loopback for additional information.	R/W	0b

Bits	Description	Type	Default
8:7	RESERVED	RO	—
6	**ALTINT** Alternate Interrupt Mode: 0 = Primary interrupt system enabled (Default) 1 = Alternate interrupt system enabled Refer to Section 3.6, Interrupt Management for additional information.	R/W	0b
5:2	RESERVED	RO	—
1	**ENERGYON** Indicates whether energy is detected. This bit transitions to “0” if no valid energy is detected within 256ms. It is reset to “1” by a hardware reset and is unaffected by a software reset. Refer to Section 3.8.3.2, Energy Detect Power-Down for additional information.	RO	1b
0	RESERVED	R/W	0b

4.2.9 SPECIAL MODES REGISTER

Index (In Decimal): 18 Size: 16 bits

Bits	Description	Type	Default
15	RESERVED	RO	—
14	MIIMODE Reflects the mode of the digital interface: 0 = MII Mode 1 = RMII Mode **Note:** When writing to this register, the default value of this bit must always be written back.	R/W NASR	Note 4-4
13:8	RESERVED	RO	—
7:5	MODE Transceiver mode of operation. Refer to Section 3.7.2, MODE[2:0]: Mode Configuration for additional details.	R/W NASR	Note 4-5
4:0	**PHYAD** PHY Address. The PHY Address is used for the SMI address and for initialization of the Cipher (Scrambler) key. Refer to Section 3.7.1, PHYAD[2:0]: PHY Address Configuration for additional details.	R/W NASR	Note 4-6

Note 4-4 The default value of this field is determined by the RMIISEL configuration strap. Refer to Section 3.7.3, RMIISEL: MII/RMII Mode Configuration for additional information.

Note 4-5 The default value of this field is determined by the MODE[2:0] configuration straps. Refer to Section 3.7.2, MODE[2:0]: Mode Configuration for additional information.

Note 4-6 The default value of this field is determined by the PHYAD[2:0] configuration straps. Refer to Section 3.7.1, PHYAD[2:0]: PHY Address Configuration for additional information.

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4.2.10 SYMBOL ERROR COUNTER REGISTER

Index (In Decimal): 26 Size: 16 bits

Bits	Description	Type	Default
15:0	SYM_ERR_CNT The symbol error counter increments whenever an invalid code symbol is received (including IDLE symbols) in 100BASE-TX mode. The counter is incremented only once per packet, even when the received packet contains more than one symbol error. This counter increments up to 65,536 (2^{16}) and rolls over to 0 after reaching the maximum value. **Note:** This register is cleared on reset, but is not cleared by reading the register. This register does not increment in 10BASE-T mode.	RO	0000h

4.2.11 SPECIAL CONTROL/STATUS INDICATIONS REGISTER

Index (In Decimal): 27 Size: 16 bits

Bits	Description	Type	Default
15	**AMDIXCTRL** HP Auto-MDIX control: 0 = Enable Auto-MDIX 1 = Disable Auto-MDIX (use 27.13 to control channel)	R/W	0b
14	RESERVED	RO	—
13	CH_SELECT Manual channel select: 0 = MDI (TX transmits, RX receives) 1 = MDIX (TX receives, RX transmits)	R/W	0b
12	RESERVED	RO	—
11	SQEOFF Disable the SQE test (Heartbeat): 0 = SQE test is enabled 1 = SQE test is disabled	R/W NASR	0b
10:5	RESERVED	RO	—
4	**XPOL** Polarity state of the 10BASE-T: 0 = Normal polarity 1 = Reversed polarity	RO	0b
3:0	RESERVED	RO	—

4.2.12 INTERRUPT SOURCE FLAG REGISTER

Index (In Decimal): 29 Size: 16 bits

Bits	Description	Type	Default
15:8	RESERVED	RO	—
7	**INT7** 0 = not source of interrupt 1 = ENERGYON generated	RO/LH	0b
6	INT6 0 = not source of interrupt 1 = Auto-Negotiation complete	RO/LH	0b
5	INT5 0 = not source of interrupt 1 = Remote Fault Detected	RO/LH	0b
4	INT4 0 = not source of interrupt 1 = Link Down (link status negated)	RO/LH	0b
3	INT3 0 = not source of interrupt 1 = Auto-Negotiation LP Acknowledge	RO/LH	0b
2	INT2 0 = not source of interrupt 1 = Parallel Detection Fault	RO/LH	0b
1	INT1 0 = not source of interrupt 1 = Auto-Negotiation Page Received	RO/LH	0b
0	**RESERVED**	RO	0b

4.2.13 INTERRUPT MASK REGISTER

Index (In Decimal): 30 Size: 16 bits

Bits	Description	Type	Default
15:8	RESERVED	RO	—
7:1	Mask Bits 0 = interrupt source is masked 1 = interrupt source is enabled **Note:** Refer to Section 4.2.12, Interrupt Source Flag Register for details on the corresponding interrupt definitions.	R/W	0000000b
0	RESERVED	RO	—

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4.2.14 PHY SPECIAL CONTROL/STATUS REGISTER

Index (In Decimal): 31 Size: 16 bits

Bits	Description	Type	Default
15:13	RESERVED	RO	—
12	Autodone Auto-negotiation done indication: 0 = Auto-negotiation is not done or disabled (or not active) 1 = Auto-negotiation is done	RO	0b
11:7	RESERVED	R/W	—
6	Enable 4B5B 0 = bypass encoder/decoder 1 = enable 4B5B encoding/decoding. MAC Interface must be configured in MII mode.	R/W	1b
5	RESERVED	RO	—
4:2	**Speed Indication** HCDSPEED value: 001 = 10BASE-T half-duplex 101 = 10BASE-T full-duplex 010 = 100BASE-TX half-duplex 110 = 100BASE-TX full-duplex	RO	XXX
1:0	RESERVED	RO	—

5.0 OPERATIONAL CHARACTERISTICS

5.1 Absolute Maximum Ratings*

Supply Voltage (VDDIO, VDD1A, VDD2A) (Note 5-1) ..... -0.5V to +3.6V

Digital Core Supply Voltage (VDDCR) (Note 5-1) ..... -0.5V to +1.5V

Ethernet Magnetics Supply Voltage ..... -0.5V to +3.6V

Positive voltage on signal pins, with respect to ground (Note 5-2) ..... +6V

Negative voltage on signal pins, with respect to ground (Note 5-3) ..... -0.5V

Positive voltage on XTAL1/CLKIN, with respect to ground ..... +3.6V

Positive voltage on XTAL2, with respect to ground ..... +2.5V

Ambient Operating Temperature in Still Air (T_A) ..... Note 5-40

Storage Temperature ..... -55°C to +150°C

Junction to Ambient (θ_{JA}) 48.3C/W

Junction to Case (θ_{JC}) ..... 10.6°C/W

Lead Temperature Range ..... Refer to JEDEC Spec. J-STD-020

HBM ESD Performance per JEDEC JESD22-A114 ..... Class 3A

IEC61000-4-2 Contact Discharge ESD Performance (Note 5-5) ..... +/-8kV

IEC61000-4-2 Air-Gap Discharge ESD Performance (Note 5-5) ..... +/-15kV

Latch-up Performance per EIA/JESD 78 ..... +/-150mA

Note 5-1 When powering this device from laboratory or system power supplies, it is important that the absolute maximum ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

Note 5-2 This rating does not apply to the following pins: XTAL1/CLKIN, XTAL2, RBIAS.

Note 5-3 This rating does not apply to the following pins: RBIAS.

Note 5-4 0°C to +85°C for extended commercial version, -40°C to +85°C for industrial version.

Note 5-5 Performed by independent 3rd party test facility.

*Stresses exceeding those listed in this section could cause permanent damage to the device. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at any condition exceeding those indicated in Section 5.2, "Operating Conditions**", Section 5.1, "Absolute Maximum Ratings*", or any other applicable section of this specification is not implied. Note, device signals are *NOT* 5 volt tolerant unless specified otherwise.

5.2 Operating Conditions**

Supply Voltage (VDDIO) ..... +1.62V to +3.6V

Analog Port Supply Voltage (VDD1A, VDD2A) ..... +3.0V to +3.6V

Digital Core Supply Voltage (VDDCR) ..... +1.08V to +1.32V

Ethernet Magnetics Supply Voltage ..... +2.25V to +3.6V

Ambient Operating Temperature in Still Air (T_A) ..... Note 5-4

**Proper operation of the device is guaranteed only within the ranges specified in this section. After the device has completed power-up, VDDIO and the magnetics power supply must maintain their voltage level with +/-10%. Varying the voltage greater than +/-10% after the device has completed power-up can cause errors in device operation.

Note: Do not drive input signals without power supplied to the device.

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5.3 Power Consumption

This section details the device power measurements taken over various operating conditions. Unless otherwise noted, all measurements were taken with power supplies at nominal values (VDDIO, VDD1A, VDD2A = 3.3V, VDDCR = 1.2V). See Section 3.8.3, Power-Down Modes for a description of the power down modes.

TABLE 5-1: DEVICE ONLY CURRENT CONSUMPTION AND POWER DISSIPATION

Power Pin Group		VDDA3.3 Power Pins(mA)	VDDCR Power Pin(mA)	VDDIO Power Pin(mA)	Total Current (mA)	Total Power (mW)
100BASE-TX /w traffic	Max	28	21	5.2	54	176
	Typical	26	18	4.3	48	158
	Min	23	18	2.4	43	101 Note 5-8
10BASE-T /w traffic	Max	10.2	12.9	0.98	24.1	79.5
	Typical	9.4	11.4	0.4	21.2	70
	Min	9.2	10.9	0.3	20.4	44 Note 5-8
Energy Detect Power Down	Max	4.5	3	0.3	7.8	25
	Typical	4.3	1.4	0.2	5.9	19.5
	Min	3.9	1.3	0	5.2	15.9 Note 5-8
General Power Down	Max	0.4	2.6	0.3	3.3	10.9
	Typical	0.3	1.2	0.2	1.7	5.6
	Min	0.3	1.1	0	1.4	2.4 Note 5-8

Note 5-6 The current at VDDCR is either supplied by the internal regulator from current entering at VDD2A, or from an external 1.2V supply when the internal regulator is disabled.

Note 5-7 Current measurements do not include power applied to the magnetics or the optional external LEDs. The Ethernet component current is typically 41mA in 100BASE-TX mode and 100mA in 10BASE-T mode, independent of the 2.5V or 3.3V supply rail of the transformer.

Note 5-8 Calculated with full flexPWR features activated: VDDIO=1.8V & internal regulator disabled.

5.4 DC Specifications

TABLE 5-2: details the non-variable I/O buffer characteristics. These buffer types do not support variable voltage operation. TABLE 5-3: details the variable voltage I/O buffer characteristics. Typical values are provided for 1.8V, 2.5V, and 3.3V VDDIO cases.

TABLE 5-2: NON-VARIABLE I/O BUFFER CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Units	Notes
IS Type Input Buffer						
Low Input Level	V_{ILI}	-0.3			V	
High Input Level	V_{IHI}			3.6	V	
Negative-Going Threshold	V_{ILT}	1.01	1.19	1.39	V	Schmitt trigger
Positive-Going Threshold	V_{IHT}	1.39	1.59	1.79	V	Schmitt trigger
Schmitt Trigger Hysteresis (V_{IHT} - V_{ILT})	V_{HYS}	336	399	459	mV	
Input Leakage (V_{IN} = VSS or VDDIO)	I_{IH}	-10		10	uA	Note 5-9
Input Capacitance	C_{IN}			2	pF	
O12 Type Buffers						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12mA
High Output Level	V_{OH}	VDD2A - 0.4			V	I_{OH} = -12mA
ICLK Type Buffer (XTAL1 Input)						Note 5-10
Low Input Level	V_{ILI}	-0.3		0.35	V	
High Input Level	V_{IHI}	0.9		3.6	V	

Note 5-9 This specification applies to all inputs and tri-stated bi-directional pins. Internal pull-down and pull-up resistors add +/- 50uA per-pin (typical).

Note 5-10 XTAL1/CLKIN can optionally be driven from a 25MHz single-ended clock oscillator.

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TABLE 5-3: VARIABLE I/O BUFFER CHARACTERISTICS

Parameter	Symbol	Min	1.8V Typ	2.5V Typ	3.3V Typ	Max	Units	Notes
VIS Type Input Buffer								
Low Input Level	V_{ILI}	-0.3					V	
High Input Level	V_{IHI}					3.6	V	
Neg-Going Threshold	V_{ILT}	0.64	0.83	1.15	1.41	1.76	V	Schmitt trigger
Pos-Going Threshold	V_{IHT}	0.81	0.99	1.29	1.65	1.90	V	Schmitt trigger
Schmitt Trigger Hysteresis (V_{IHT} - V_{ILT})	V_{HYS}	102	158	136	138	288	mV	
Input Leakage (V_{IN} = VSS or VDDIO)	I_{IH}	-10				10	uA	Note 5-11
Input Capacitance	C_{IN}					2	pF	
VO8 Type Buffers								
Low Output Level	V_{OL}					0.4	V	I_{OL} = 8mA
High Output Level	V_{OH}	VDDIO - 0.4					V	I_{OH} = -8mA
VOD8 Type Buffer								
Low Output Level	V_{OL}					0.4	V	I_{OL} = 8mA

Note 5-11 This specification applies to all inputs and tri-stated bi-directional pins. Internal pull-down and pull-up resistors add +/- 50uA per-pin (typical).

TABLE 5-4: 100BASE-TX TRANSCEIVER CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Units	Notes
Peak Differential Output Voltage High	V_{PPH}	950	—	1050	mVpk	Note 5-12
Peak Differential Output Voltage Low	V_{PPL}	-950	—	-1050	mVpk	Note 5-12
Signal Amplitude Symmetry	V_{SS}	98	—	102	%	Note 5-12
Signal Rise and Fall Time	T_{RF}	3.0	—	5.0	nS	Note 5-12
Rise and Fall Symmetry	T_{RFS}	—	—	0.5	nS	Note 5-12
Duty Cycle Distortion	D_{CD}	35	50	65	%	Note 5-13
Overshoot and Undershoot	V_{OS}	—	—	5	%	—
Jitter	—	—	—	1.4	nS	Note 5-14

Note 5-12 Measured at line side of transformer, line replaced by 100Ω (+/- 1%) resistor.

Note 5-13 Offset from 16nS pulse width at 50% of pulse peak.

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Note 5-14 Measured differentially.

TABLE 5-5: 10BASE-T TRANSCEIVER CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Units	Notes
Transmitter Peak Differential Output Voltage	V_{OUT}	2.2	2.5	2.8	V	Note 5-15
Receiver Differential Squelch Threshold	V_{DS}	300	420	585	mV	—

Note 5-15 Min/max voltages guaranteed as measured with 100Ω resistive load.

5.5 AC Specifications

This section details the various AC timing specifications of the device.

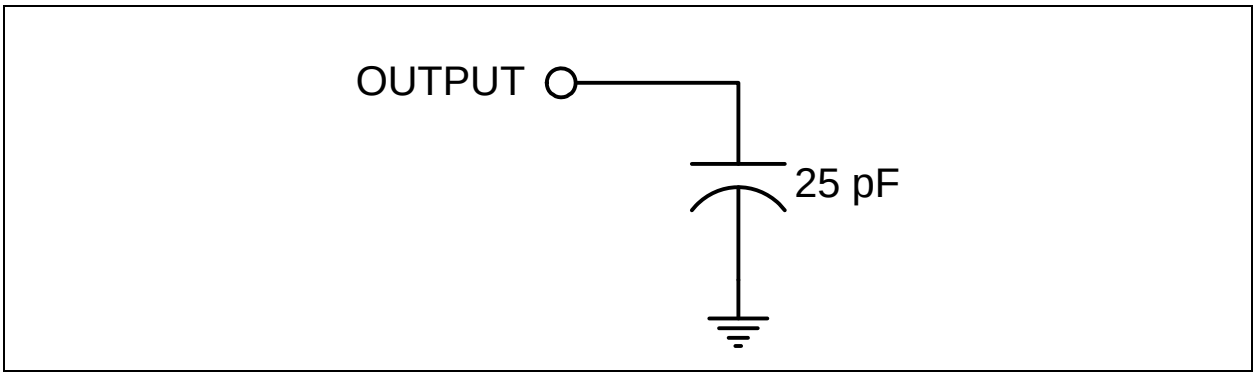
Note 5-16 The MII/SMI timing adheres to the IEEE 802.3 specification. Refer to the IEEE 802.3 specification for additional timing information.

Note 5-17 The RMII timing adheres to the RMII Consortium RMII Specification R1.2.

5.5.1 EQUIVALENT TEST LOAD

Output timing specifications assume a 25pF equivalent test load, unless otherwise noted, as illustrated in Figure 5-1 below.

FIGURE 5-1: OUTPUT EQUIVALENT TEST LOAD



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5.5.2 POWER SEQUENCE TIMING

This diagram illustrates the device power sequencing requirements. The VDDIO, VDD1A, VDD2A and magnetics power supplies can turn on in any order provided they all reach operational levels within the specified time period t_{pon}. Device power supplies can turn off in any order provided they all reach 0 volts within the specified time period p_{off}.

FIGURE 5-2: POWER SEQUENCE TIMING

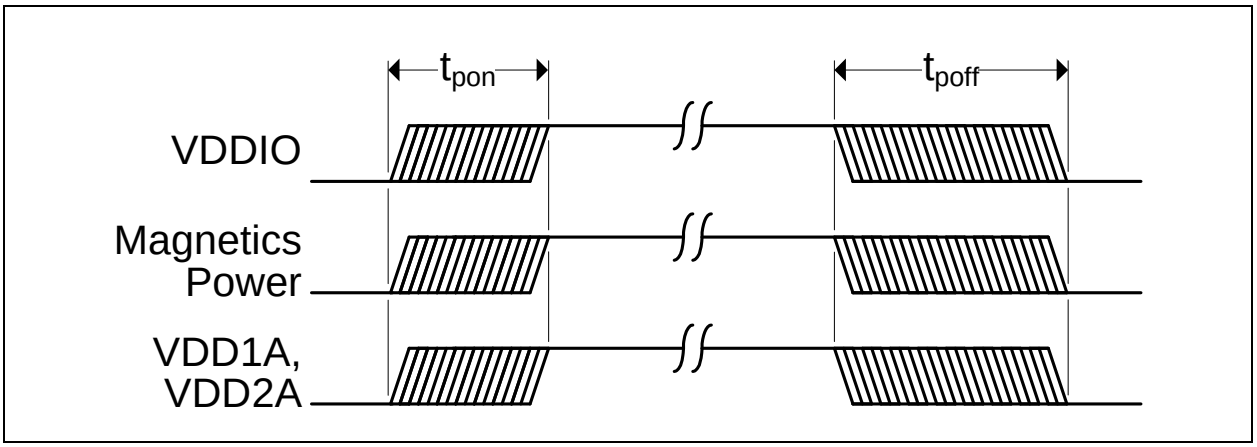


TABLE 5-6: POWER SEQUENCE TIMING VALUES

Symbol	Description	Min	Typ	Max	Units
t_{pon}	Power supply turn on time	—	—	50	mS
t_{poff}	Power supply turn off time	—	—	500	mS

Note: When the internal regulator is disabled, a power-up sequencing relationship exists between VDDCR and the 3.3V power supply. For additional information refer to Section 3.7.4, REGOFF: Internal +1.2V Regulator Configuration.

5.5.3 POWER-ON NRST & CONFIGURATION STRAP TIMING

This diagram illustrates the nRST reset and configuration strap timing requirements in relation to power-on. A hardware reset (nRST assertion) is required following power-up. For proper operation, nRST must be asserted for no less than t_{rstia}. The nRST pin can be asserted at any time, but must not be deasserted before t_{purstd} after all external power supplies have reached 80% of their nominal operating levels. In order for valid configuration strap values to be read at power-up, the t_{css} and t_{csh} timing constraints must be followed. Refer to Section 3.8.5, Resets for additional information.

FIGURE 5-3: POWER-ON NRST & CONFIGURATION STRAP TIMING

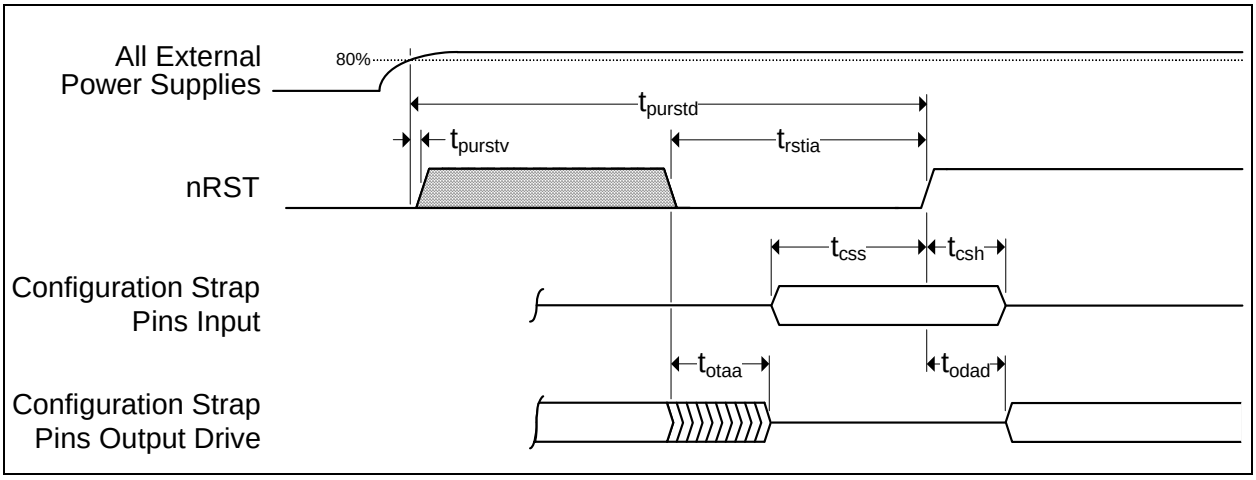


TABLE 5-7: POWER-ON NRST & CONFIGURATION STRAP TIMING VALUES

symbol	DESCRIPTION	min	typ	max	units
t_{purstd}	External power supplies at 80% to nRST deassertion	25	—	—	mS
t_{purstv}	External power supplies at 80% to nRST valid	0	—	—	nS
t_{rstia}	nRST input assertion time	100	—	—	µS
t_{css}	Configuration strap pins setup to nRST deassertion	200	—	—	nS
t_{csh}	Configuration strap pins hold after nRST deassertion	1	—	—	nS
t_{otaa}	Output tri-state after nRST assertion		—	50	nS
t_{odad}	Output drive after nRST deassertion	2	—	800 (Note 5-20)	nS

Note 5-18 nRST deassertion must be monotonic.

Note 5-19 Device configuration straps are latched as a result of nRST assertion. Refer to Section 3.7, Configuration Straps for details. Configuration straps must only be pulled high or low and must not be driven as inputs.

Note 5-20 20 clock cycles for 25MHz, or 40 clock cycles for 50MHz.

5.5.4 MII INTERFACE TIMING

This section specifies the MII interface transmit and receive timing. Please refer to Section 3.4.1, MII for additional details.

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FIGURE 5-4: MII RECEIVE TIMING

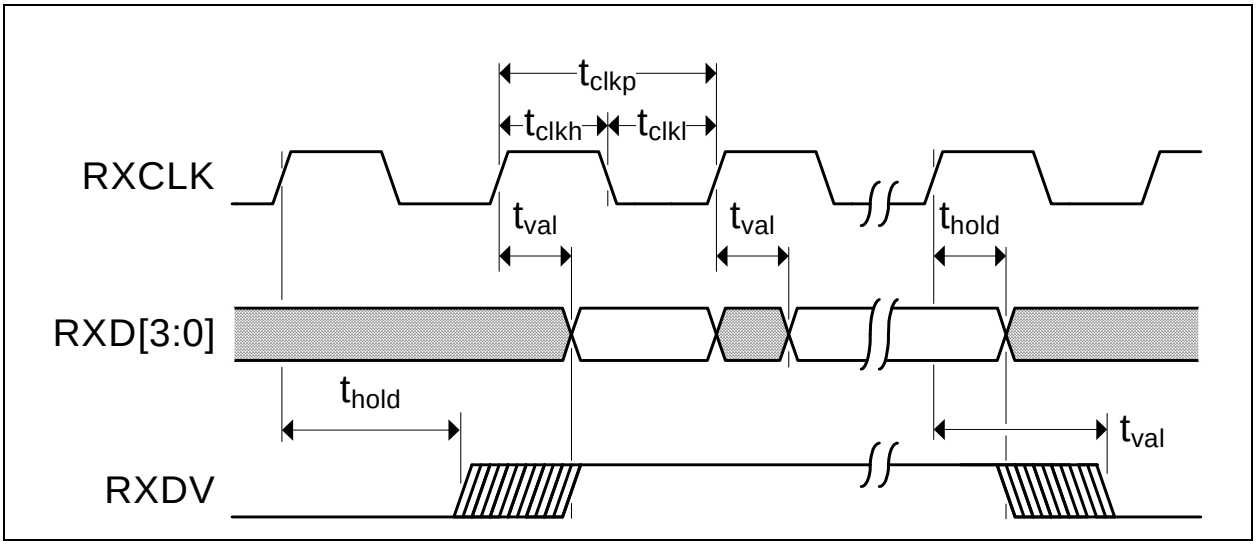


Table 1.1 MII Receive Timing Values

SYMBOL	DESCRIPTION	MIN	MAX	UNITS	NOTES
t_{clkp}	RXCLK period	Note 5-21	—	ns	
t_{clkh}	RXCLK high time	t_{clkp}*0.4	t_{clkp}*0.6	ns	
t_{clkl}	RXCLK low time	t_{clkp}*0.4	t_{clkp}*0.6	ns	
t_{val}	RXD[3:0], RXDV output valid from rising edge of RXCLK		28.0	ns	Note 5-22
t_{hold}	RXD[3:0], RXDV output hold from rising edge of RXCLK	10.0	—	ns	Note 5-22

Note 5-21 40ns for 100BASE-TX operation, 400ns for 10BASE-T operation.

Note 5-22 Timing was designed for system load between 10 pf and 25 pf.

FIGURE 5-5: MII TRANSMIT TIMING

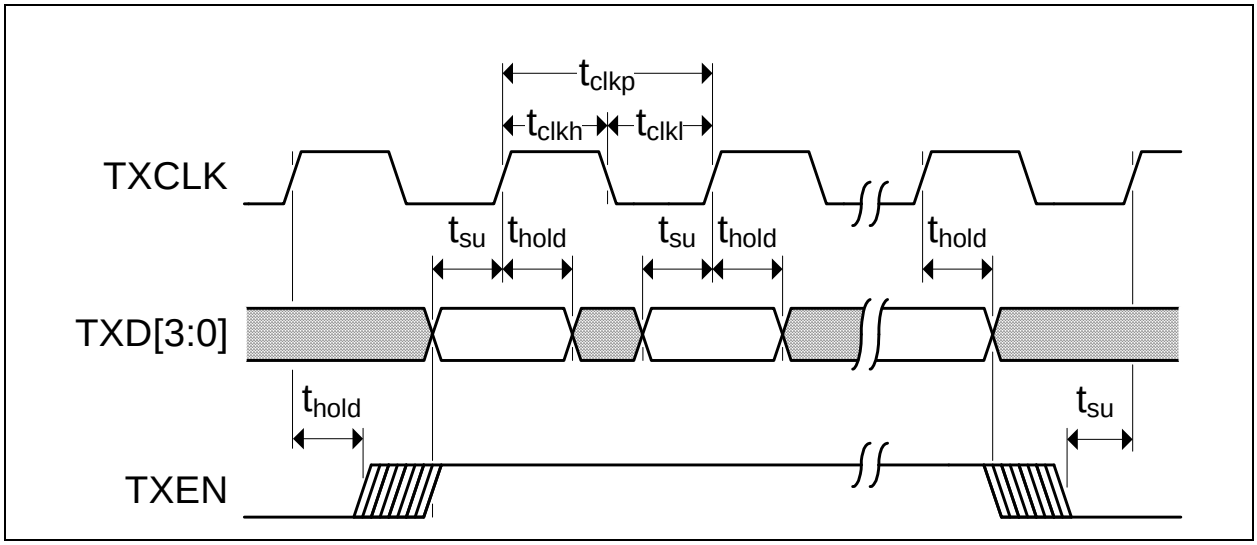


TABLE 5-8: MII TRANSMIT TIMING VALUES

SYMBOL	DESCRIPTION	MIN	MAX	UNITS	NOTES
t_{clkp}	TXCLK period	Note 5-23	—	ns	—
t_{clkh}	TXCLK high time	t_{clkp}*0.4	t_{clkp}*0.6	ns	—
t_{clkl}	TXCLK low time	t_{clkp}*0.4	t_{clkp}*0.6	ns	—
t_{su}	TXD[3:0], TXEN setup time to rising edge of TXCLK	12.0	—	ns	Note 5-24
t_{hold}	TXD[3:0], TXEN hold time after rising edge of TXCLK	0	—	ns	Note 5-24

Note 5-23 40ns for 100BASE-TX operation, 400ns for 10BASE-T operation.

Note 5-24 Timing was designed for system load between 10 pf and 25 pf.

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5.5.5 RMII INTERFACE TIMING

FIGURE 5-6: RMII TIMING

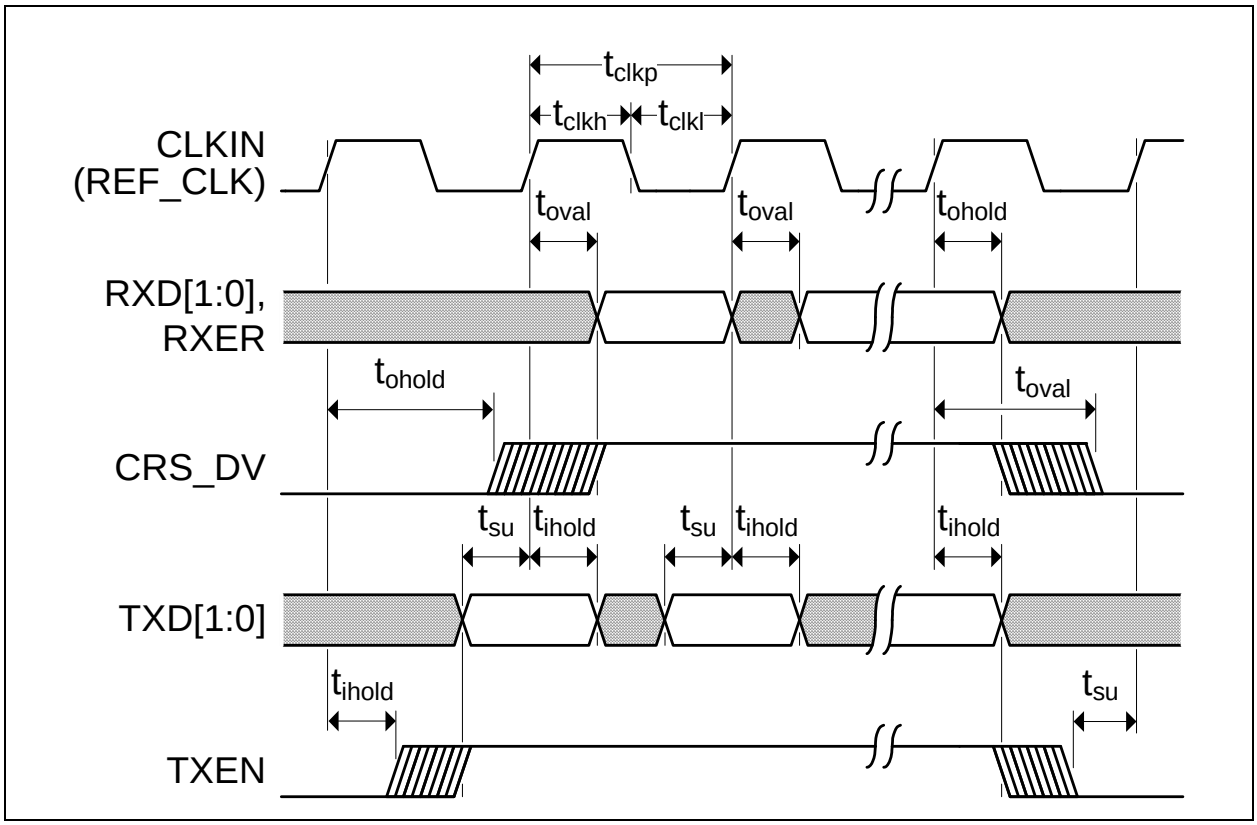


TABLE 5-9: RMII TIMING VALUES

Symbol	Description	Min	Max	Units	Notes
t_{clkp}	CLKIN period	20	—	ns	—
t_{clkh}	CLKIN high time	t_{clkp}*0.35	t_{clkp}*0.65	ns	—
t_{clkl}	CLKIN low time	t_{clkp}*0.35	t_{clkp}*0.65	ns	—
t_{oval}	RXD[1:0], RXER, CRS_DV output valid from rising edge of CLKIN	—	14.0	ns	Note 5-25
t_{ohold}	RXD[1:0], RXER, CRS_DV output hold from rising edge of CLKIN	3.0	—	ns	Note 5-25
t_{su}	TXD[1:0], TXEN setup time to rising edge of CLKIN	4.0	—	ns	Note 5-25
t_{ihold}	TXD[1:0], TXEN input hold time after rising edge of CLKIN	1.5	—	ns	Note 5-25

Note 5-25 Timing was designed for system load between 10 pf and 25 pf.

5.5.5.1 RMII CLKIN Requirements

TABLE 5-10: RMII CLKIN (REF_CLK) TIMING VALUES

Parameter	Min	Typ	Max	Units	Notes
CLKIN frequency		50	—	MHz	—
CLKIN Frequency Drift		—	± 50	ppm	—
CLKIN Duty Cycle	40	—	60	%	—
CLKIN Jitter		—	150	psec	p-p – not RMS

5.5.6 SMI TIMING

This section specifies the SMI timing of the device. Please refer to Section 3.5, Serial Management Interface (SMI) for additional details.

FIGURE 5-7: SMI TIMING

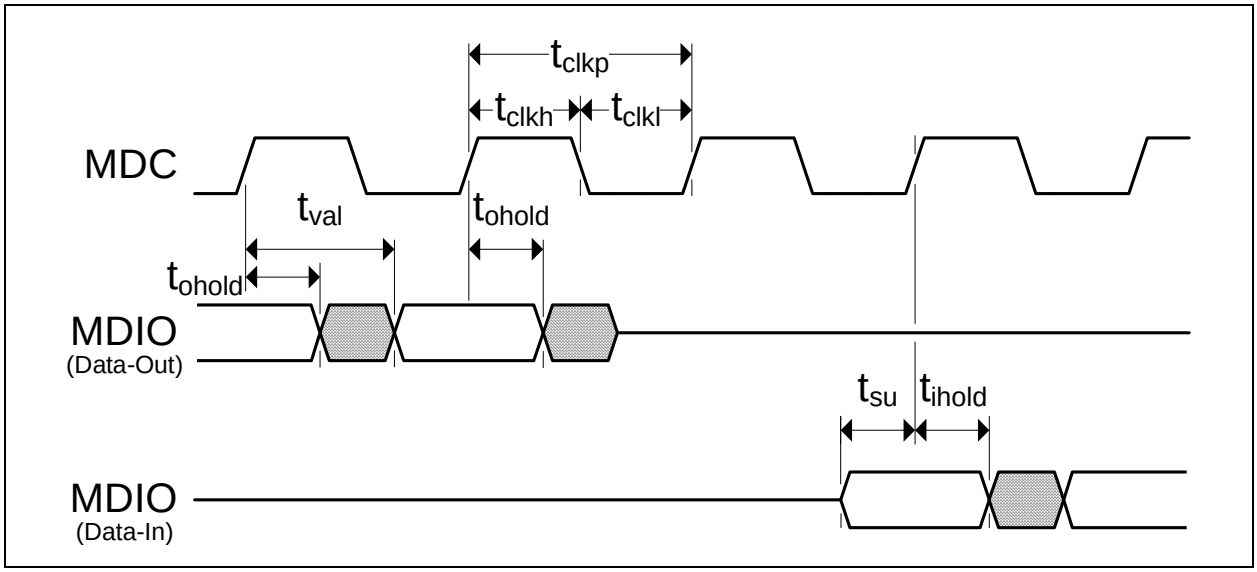


TABLE 5-11: SMI TIMING VALUES

Symbol	Description	Min	Max	Units	Notes
t_{clkp}	MDC period	400	—	ns	—
t_{clkh}	MDC high time	160 (80%)	—	ns	—
t_{clkl}	MDC low time	160 (80%)	—	ns	—
t_{val}	MDIO (read from PHY) output valid from rising edge of MDC	—	300	ns	—
t_{ohold}	MDIO (read from PHY) output hold from rising edge of MDC	0	—	ns	—
t_{su}	MDIO (write to PHY) setup time to rising edge of MDC	10	—	ns	—
t_{ihold}	MDIO (write to PHY) input hold time after rising edge of MDC	10	—	ns	—

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5.6 Clock Circuit

The device can accept either a 25MHz crystal (preferred) or a 25MHz single-ended clock oscillator (±50ppm) input. If the single-ended clock oscillator method is implemented, XTAL2 should be left unconnected and XTAL1/CLKIN should be driven with a nominal 0-3.3V clock signal.

It is recommended that a crystal utilizing matching parallel load capacitors be used for the crystal input/output signals (XTAL1/XTAL2). Either a 300uW or 100uW 25MHz crystal may be utilized. The 300uW 25MHz crystal specifications are detailed in Section 5.6.1, "300uW 25MHz Crystal Specification," on page 65. The 100uW 25MHz crystal specifications are detailed in Section 5.6.2, "100uW 25MHz Crystal Specification," on page 66.

5.6.1 300UW 25MHZ CRYSTAL SPECIFICATION

When utilizing a 300uW 25MHz crystal, the following circuit design (Figure 5-8) and specifications (Table 5-12) are required to ensure proper operation.

FIGURE 5-8: 300UW 25MHZ CRYSTAL CIRCUIT

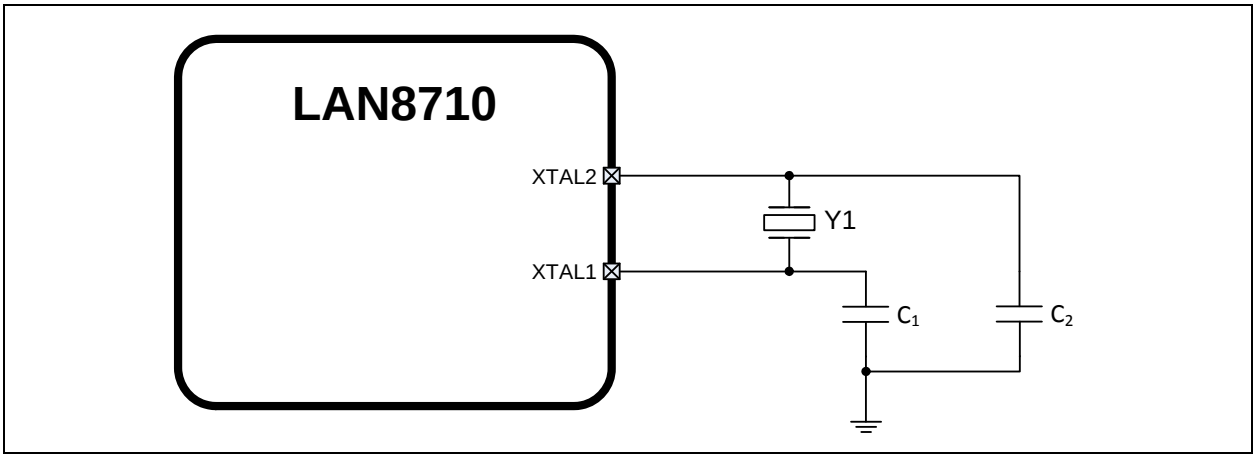


TABLE 5-12: 300UW 25MHZ CRYSTAL SPECIFICATIONS

Parameter	Symbol	Min	Nom	Max	Units	Notes
Crystal Cut	AT, typ					—
Crystal Oscillation Mode	Fundamental Mode					—
Crystal Calibration Mode	Parallel Resonant Mode					—
Frequency	F_{fund}	—	25.000	—	MHz	—
Frequency Tolerance @ 25°C	F_{tol}	—	—	±50	PPM	Note 5-26
Frequency Stability Over Temp	F_{temp}	—	—	±50	PPM	Note 5-26
Frequency Deviation Over Time	F_{age}	—	+/-3 to 5	—	PPM	Note 5-27
Total Allowable PPM Budget	—	—	—	±50	PPM	Note 5-28
Shunt Capacitance	C_O	—	7 typ	—	pF	—
Load Capacitance	C_L	—	20 typ	—	pF	—
Drive Level	P_W	300	—	—	uW	—
Equivalent Series Resistance	R_1	—	—	30	Ohm	—
Operating Temperature Range	—	Note 5-35	—	+85	°C	—
XTAL1/CLKIN Pin Capacitance	—	—	3 typ	—	pF	Note 5-30
XTAL2 Pin Capacitance	—	—	3 typ	—	pF	Note 5-30

Note 5-26 The maximum allowable values for Frequency Tolerance and Frequency Stability are application dependent. Since any particular application must meet the IEEE ±50 PPM Total PPM Budget, the combination of these two values must be approximately ±45 PPM (allowing for aging).

Note 5-27 Frequency Deviation Over Time is also referred to as Aging.

Note 5-28 The total deviation for the Transmitter Clock Frequency is specified by IEEE 802.3u as ±100 PPM.

Note 5-29 0°C for extended commercial version, -40°C for industrial version.

Note 5-30 This number includes the pad, the bond wire and the lead frame. PCB capacitance is not included in this value. The XTAL1/CLKIN pin, XTAL2 pin and PCB capacitance values are required to accurately calculate the value of the two external load capacitors. The total load capacitance must be equivalent to what the crystal expects to see in the circuit so that the crystal oscillator will operate at 25.000 MHz.

5.6.2 100UW 25MHZ CRYSTAL SPECIFICATION

When utilizing a 100uW 25MHz crystal, the following circuit design (Figure 5-9) and specifications (Table 5-13) are required to ensure proper operation.

FIGURE 5-9: 100UW 25MHZ CRYSTAL CIRCUIT

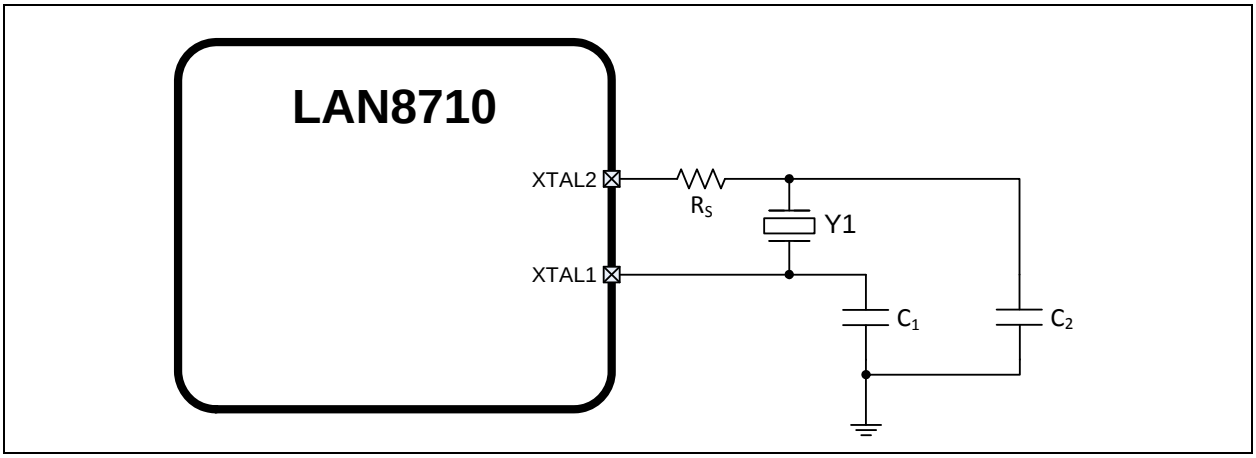


TABLE 5-13: 100UW 25MHZ CRYSTAL SPECIFICATIONS

Parameter	Symbol	Min	Nom	Max	Units	Notes
Crystal Cut	AT, typ					—
Crystal Oscillation Mode	Fundamental Mode					—
Crystal Calibration Mode	Parallel Resonant Mode					—
Frequency	F_{fund}	—	25.000	—	MHz	—
Frequency Tolerance @ 25°C	F_{tol}	—	—	±50	PPM	Note 5-31
Frequency Stability Over Temp	F_{temp}	—	—	±50	PPM	Note 5-31
Frequency Deviation Over Time	F_{age}	—	±3 to 5	—	PPM	Note 5-32
Total Allowable PPM Budget	—	—	—	±50	PPM	Note 5-33
Shunt Capacitance	C_O	—	—	5	pF	—
Load Capacitance	C_L	8	—	12	pF	—
Drive Level	P_W	—	100	—	uW	Note 5-34

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TABLE 5-13: 100UW 25MHZ CRYSTAL SPECIFICATIONS (CONTINUED)

Parameter	Symbol	Min	Nom	Max	Units	Notes
Equivalent Series Resistance	R_1	—	—	80	Ohm	—
XTAL2 Series Resistor	R_s	495	500	505	Ohm	—
Operating Temperature Range	—	Note 5-35	—	+85	^oC	—
XTAL1/CLKIN Pin Capacitance	—	—	3 typ	—	pF	Note 5-36
XTAL2 Pin Capacitance	—	—	3 typ	—	pF	Note 5-36

Note 5-31 The maximum allowable values for Frequency Tolerance and Frequency Stability are application dependent. Since any particular application must meet the IEEE ±50 PPM Total PPM Budget, the combination of these two values must be approximately ±45 PPM (allowing for aging).

Note 5-32 Frequency Deviation Over Time is also referred to as Aging.

Note 5-33 The total deviation for the Transmitter Clock Frequency is specified by IEEE 802.3u as ±100 PPM.

Note 5-34 The crystal must support 100uW operation to utilize this circuit.

Note 5-35 0^oC for extended commercial version, -40^oC for industrial version.

Note 5-36 This number includes the pad, the bond wire and the lead frame. PCB capacitance is not included in this value. The XTAL1/CLKIN pin, XTAL2 pin and PCB capacitance values are required to accurately calculate the value of the two external load capacitors. The total load capacitance must be equivalent to what the crystal expects to see in the circuit so that the crystal oscillator will operate at 25.000 MHz.

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6.0 PACKAGE INFORMATION

6.1 32-QFN (Punch)

FIGURE 6-1: 32-QFN PACKAGE

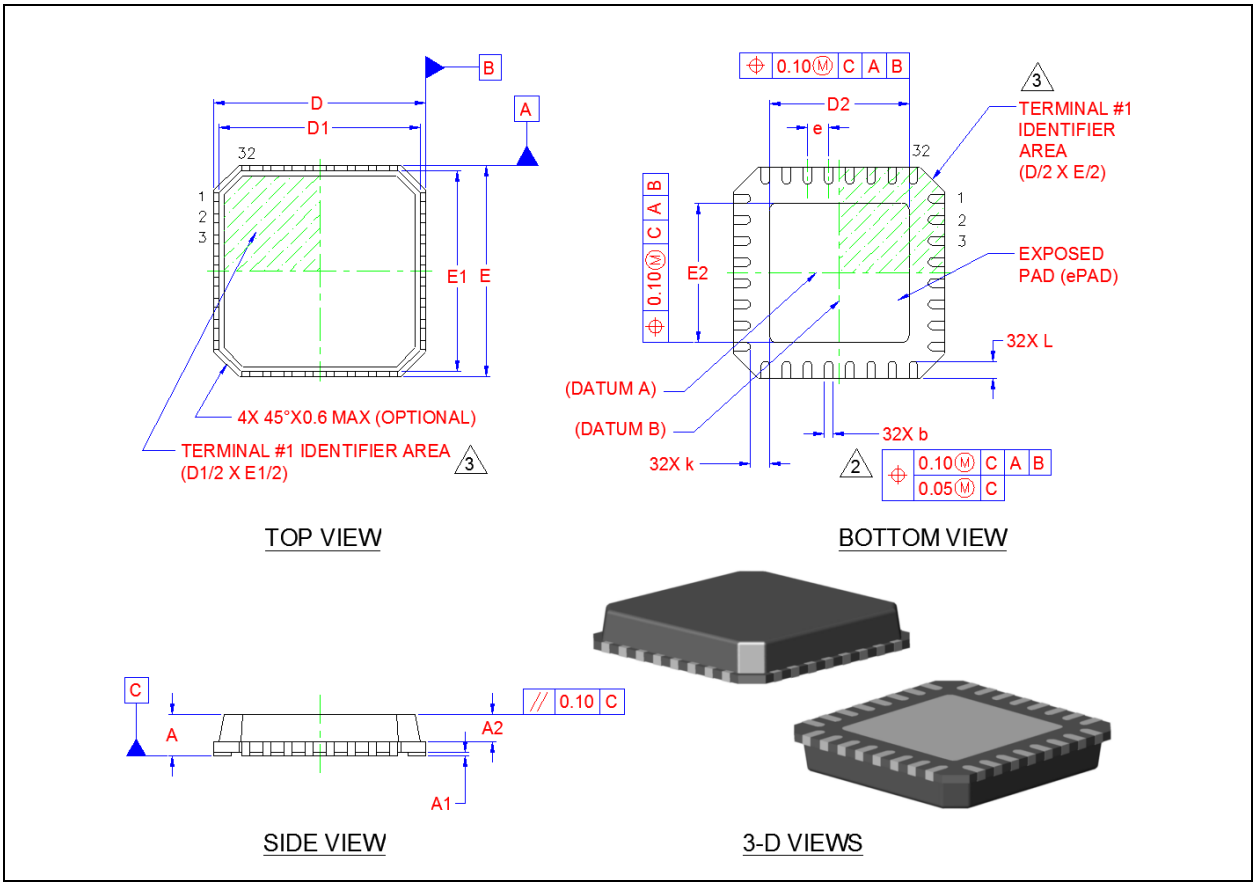


TABLE 6-1: 32-QFN DIMENSIONS

	Min	Nominal	Max	Remarks
A	0.70	0.85	1.00	Overall Package Height
A1	0	0.02	0.05	Standoff
A2	—	0.65	0.90	Mold Cap Thickness
D/E	4.90	5.00	5.10	X/Y Body Size
D1/E1	4.55	4.75	4.95	X/Y Mold Cap Size
D2/E2	3.20	3.30	3.40	X/Y Exposed Pad Size
L	0.30	0.40	0.50	Terminal Length
b	0.18	0.25	0.30	Terminal Width
k	0.35	0.45	—	Terminal to Exposed Pad Clearance
e		0.50 BSC		Terminal Pitch

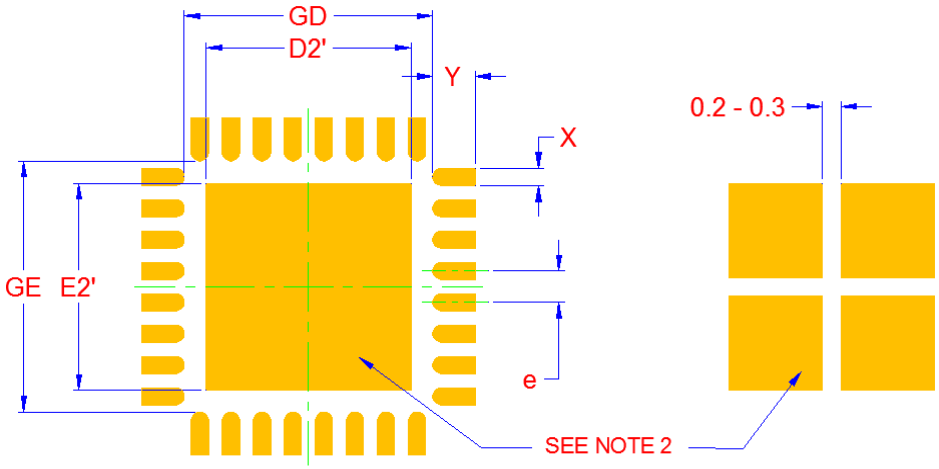
Note 1: All dimensions are in millimeters unless otherwise noted.

2: Dimension “b” applies to plated terminals and is measured between 0.15 and 0.30 mm from the terminal tip.

3: The pin 1 identifier may vary, but is always located within the zone indicated.

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FIGURE 6-2: 32-QFN RECOMMENDED PCB LAND PATTERN

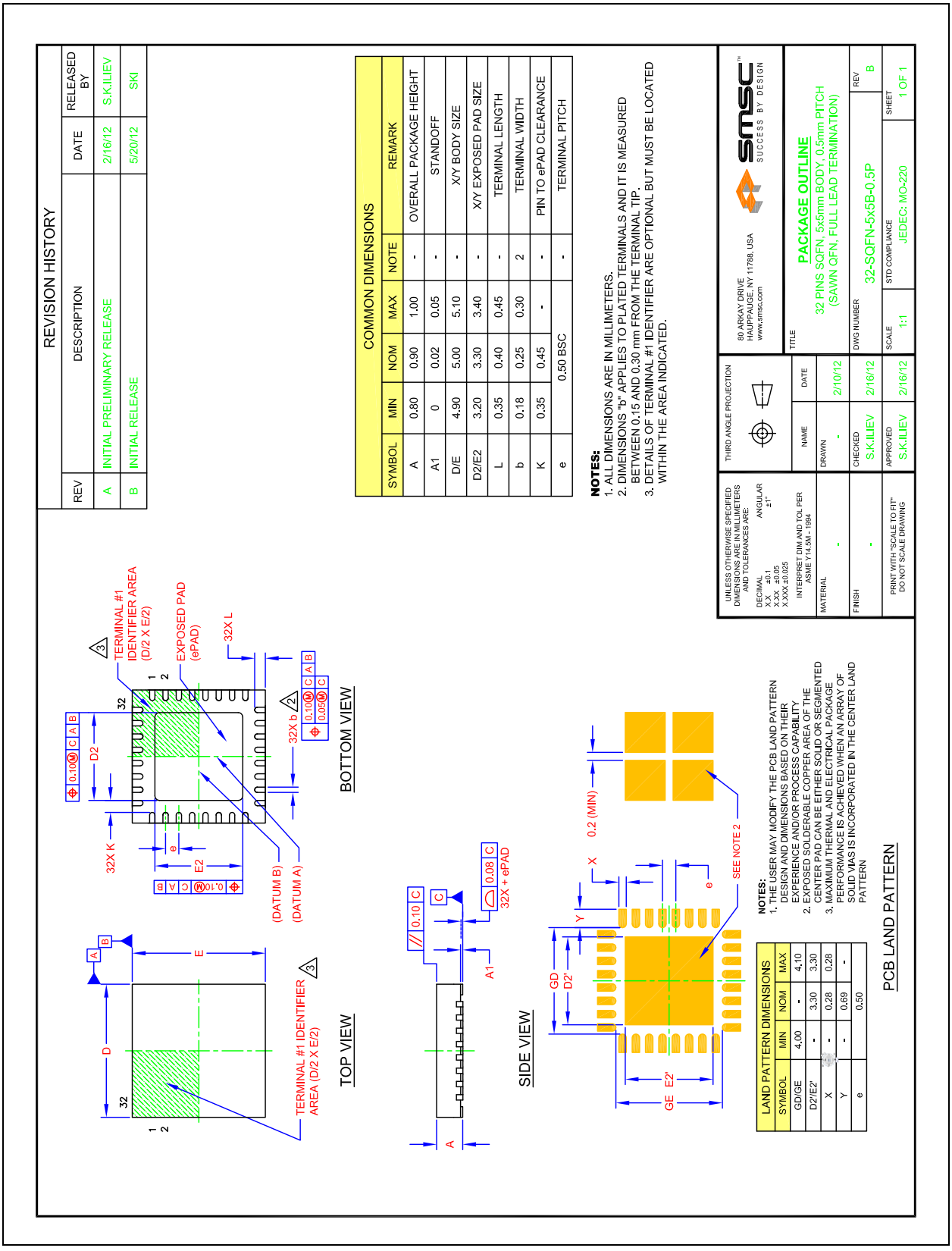


LAND PATTERN DIMENSIONS			
SYMBOL	MIN	NOM	MAX
GD/GE	4.00	-	4.10
D2'/E2'	3.10	-	3.30
X	-	0.24	0.28
Y	-	0.69	0.75
e		0.50	

NOTES:
1. THE USER MAY MODIFY THE PCB LAND PATTERN DESIGN AND DIMENSIONS BASED ON THEIR EXPERIENCE AND/OR PROCESS CAPABILITY
2. EXPOSED SOLDERABLE COPPER AREA OF THE CENTER PAD CAN BE EITHER SOLID OR SEGMENTED
3. MAXIMUM THERMAL AND ELECTRICAL PACKAGE PERFORMANCE IS ACHIEVED WHEN AN ARRAY OF SOLID VIAS IS INCORPORATED IN THE CENTER LAND PATTERN

6.2 32-SQFN (Sawn)

FIGURE 6-3: 32-SQFN PACKAGE



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6.3 Tape & Reel Information

FIGURE 6-4: TAPING DIMENSIONS AND PART ORIENTATION

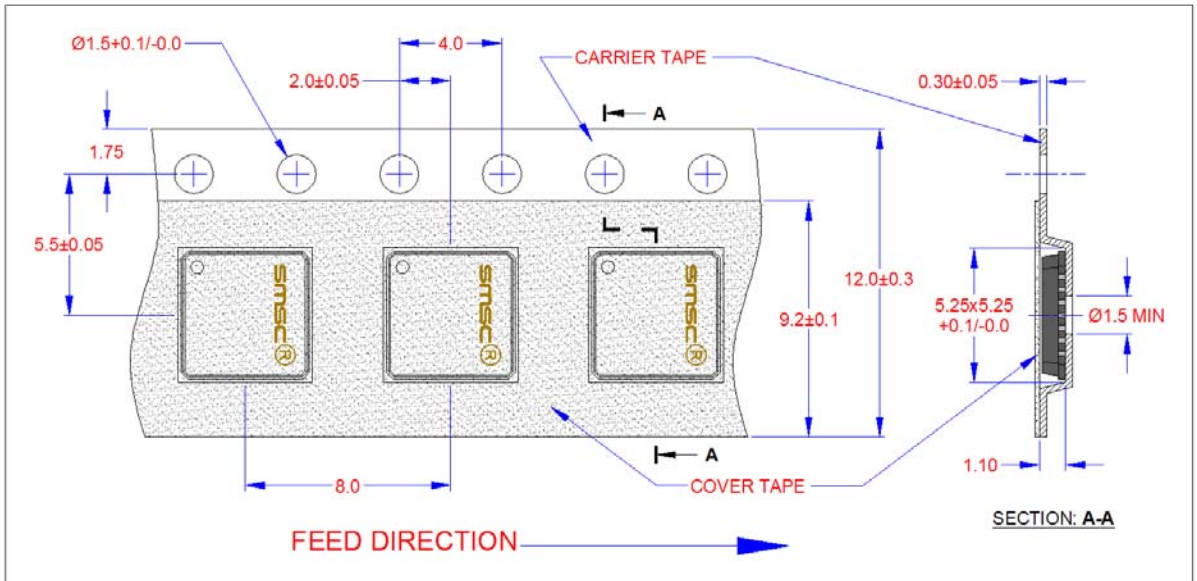
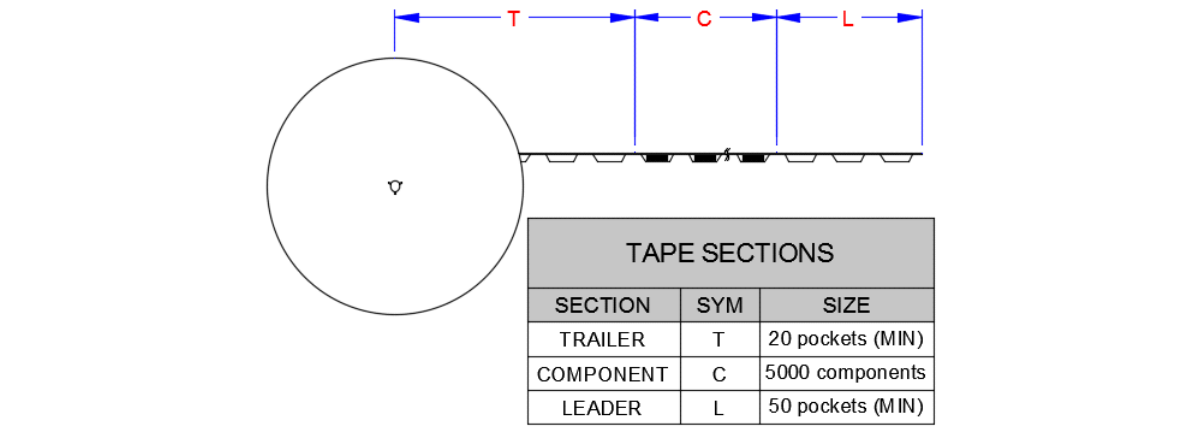


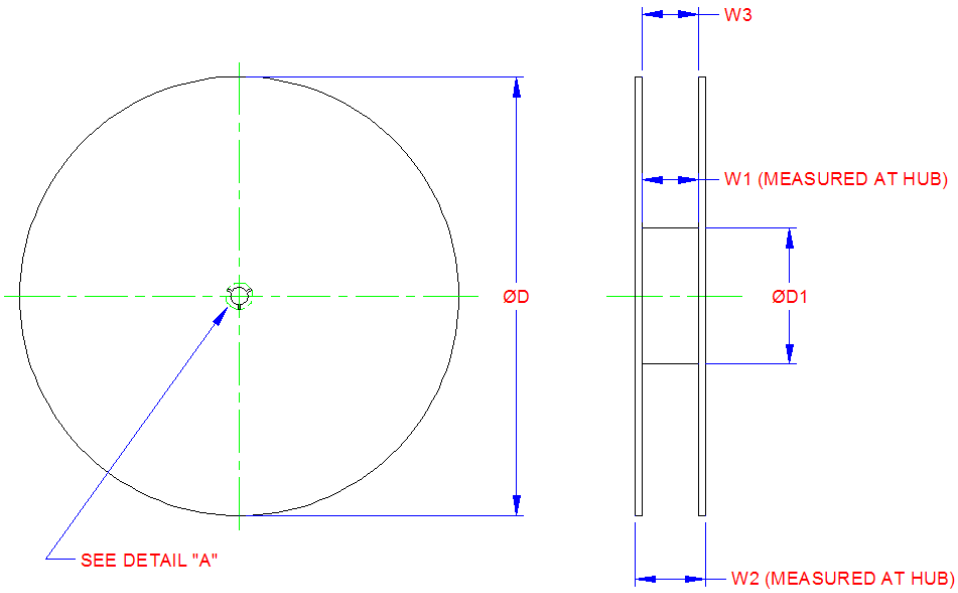
FIGURE 6-5: TAPE LENGTH AND PART QUANTITY

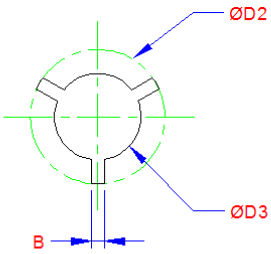


TAPE SECTIONS		
SECTION	SYM	SIZE
TRAILER	T	20 pockets (MIN)
COMPONENT	C	5000 components
LEADER	L	50 pockets (MIN)

Note: Standard reel size is 5,000 pieces per reel.

FIGURE 6-6: REEL DIMENSIONS





DETAIL "A"

REEL DIMs for 12mm CARRIER TAPE			
PART	FEATURE	SYM	SIZE (mm)
FLANGE	DIAMETER	D	330 (+0.25/-4.00)
	SPACE between FLANGES	W1	12.4 (+2.0/-0.0)
	OVERALL WITH	W2	18.4 (MAX)
	MIN SPACE "W1" AT FLANGE EDGE	W3	12.3 (MIN)
HUB	OUTER DIAMETER	D1	102 REF
	KEY SLIT DIAMETER	D2	20.2 (MIN)
	ARBOR HOLE DIAMETER	D3	13.0 (+0.5/-0.2)
	KEY SLIT WIDTH	B	2.0 (±0.5)

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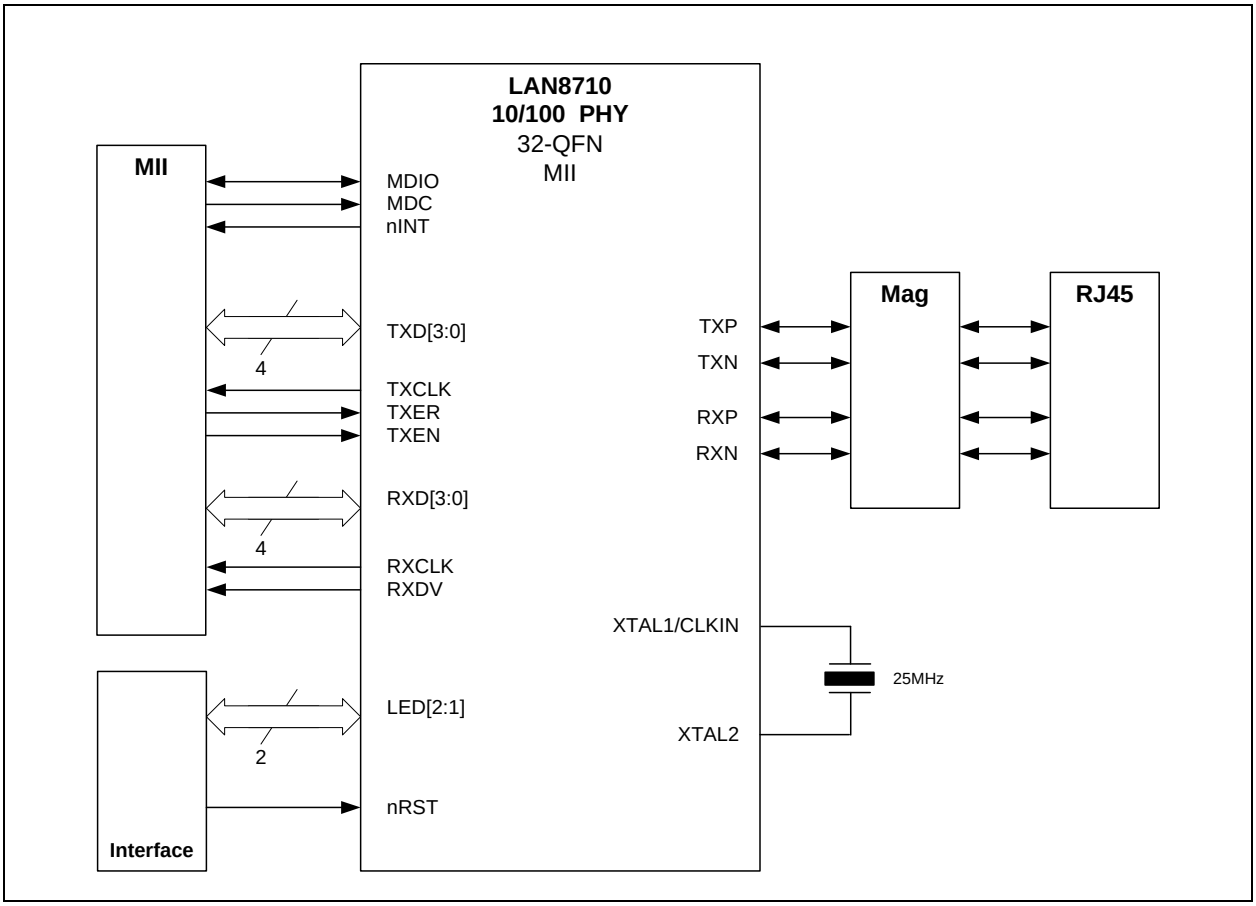
7.0 APPLICATION NOTES

7.1 Application Diagram

The device requires few external components. The voltage on the magnetics center tap can range from 2.5 - 3.3V.

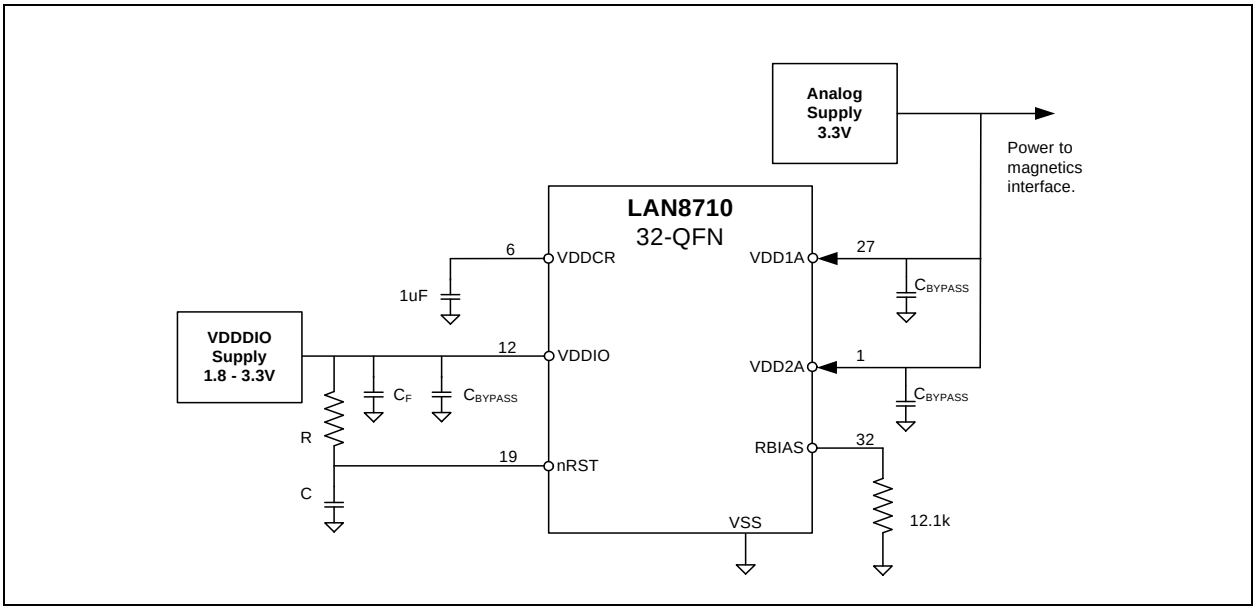
7.1.1 MII DIAGRAM

FIGURE 7-1: SIMPLIFIED APPLICATION DIAGRAM



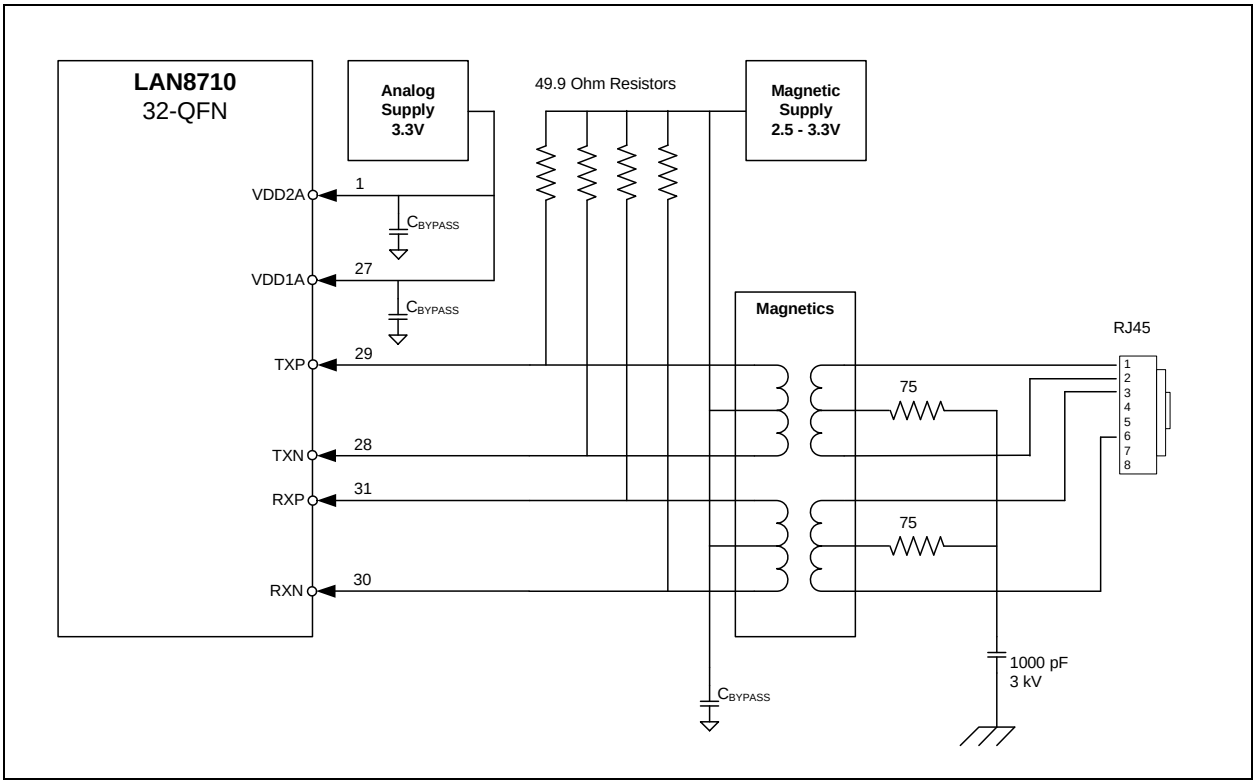
7.1.2 POWER SUPPLY DIAGRAM

FIGURE 7-2: HIGH-LEVEL SYSTEM DIAGRAM FOR POWER



7.1.3 TWISTED-PAIR INTERFACE DIAGRAM

FIGURE 7-4: COPPER INTERFACE DIAGRAM



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APPENDIX A: DATA SHEET REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision	Section/Figure/Entry	Correction
Rev B. (07-15-16)	Section 5.1, "Absolute Maximum Ratings*," on page 54	Update to Positive voltage on XTAL1/CLKIN, with respect to ground.
	Table 5-2, “Non-Variable I/O Buffer Characteristics,” on page 56	Update to min/max values for the last row, ICLK Type Buffer (XTAL1 Input) - High Input Level.
Rev. A (06-24-16)	All	Document converted to Microchip look and feel. Replaces SMSC Rev. 1.4 (08-23-12).
	Section 5.2, "Operating Conditions**," on page 54	Increased VDDCR operational limits from “+1.14V to +1.26V” to “+1.08V to +1.32V”
	Section 5.6, "Clock Circuit," on page 65	Added new 100uW crystal specifications and circuit diagram. The section is now split into two subsections, one for 300uW crystals and the other for 100uW crystals.
	Section 6.0, "Package Information," on page 68	Added new subsections to include SQFN package information.
	Section , "Product Identification System," on page 77	Updated ordering codes with sawn SQFN package options.
Rev. 1.4 (08-23-12)	Section 4.2.2, Basic Status Register	Updated definitions of bits 10:8.
	Section 4.2.14, "PHY Special Control/Status Register," on page 53	Updated bit 6 definition.
	Cover	Ordering information modified.
Rev. 1.3 (04-20-11)	Cover	Added copper bond wire ordering codes to LAN8710 ordering codes
	Table 4.2.9, “Special Modes Register,” on page 50	Updated MIIMODE bit description and added note: “When writing to this register the default value of this bit must always be written back.”
	Section 3.7.3, "RMIISEL: MII/RMII Mode Configuration," on page 31	Updated second paragraph to: “When the nRST pin is deasserted, the MIIMODE bit of the Special Modes Register is loaded according to the RMIISEL configuration strap. The mode is reflected in the MIIMODE bit of the Special Modes Register.”
	Section 3.8.9.2, "Far Loopback," on page 36	Updated section to defeature information about register control of the MII/RMII mode.
Rev. 1.2 (11-10-10)	Section 5.5.5, "RMII Interface Timing," on page 63	Updated diagrams and tables to include RXER.

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X]	-	[X](1)	-	[XXX]
Device	Temperature Range		Tape & Reel Option		Package

Device:	LAN8710A	
Temperature Range:	-EZC = 0°C to +85°C	(Extended Commercial)
	i-EZK = -40°C to +85°C	(Industrial)
Tape and Reel Option:	Blank = Standard packaging (tray)	
	TR = Tape and Reel(1)	
Package:	Blank = Punch Package (32-QFN)	
	ABC = Sawn Package (32-SQFN)	

Examples:

a) LAN8710Ai-EZK-TR
Industrial temp., Tape & Reel, 32-QFN (Punch)

b) LAN8710A-EZC-ABC
Ext. commercial temp., Tray, 32-SQFN (Sawn)

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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